Advanced Packaging Technology for Leading Edge Microelectronics and Flexible Electronics

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Presentation Objective

This presentation will explore advanced packaging solutions for next generation microelectronics in key applications areas.

We will look at how semiconductor trends and key market segments are driving advanced microelectronics packaging developments.

Finally, we will look at some approaches to and issues with organic and inorganic flexible electronics.
GE Global Research
Advanced Packaging Technologies

- Fine Line Multilayer Flex
- Thin Film Passives
- Multichip Modules
- 3D Electronic Assembly
- Chip Scale Packaging
- LED Packaging

- Power Packaging
- Power Overlay Packaging
- WBG Packaging
- Nano Interconnects
- MEMS Packaging
- Photonics Packaging

Packaging & Interconnection Development, Prototype and Low Volume Production Fabrication, Assembly and Test Capability.
GRC Advanced Packaging Technologies

Flex Circuits

Sensor/MEMS

Floating Pads

High Speed Digital MCM
GRC Advanced Packaging Technologies

A/D Mixed MCM

Photonics

Power Converter

3-D Micro Stack
Evolving Microelectronics Technologies:

Gordon Moore’s observation 1965, every 18 months:

• 2x increase in gate count
• 1.5x increase in I/O count

Still following Moore’s Law today due to semiconductor trends in:

• feature size reduction
• innovative structures
• supply voltage reductions
The Semiconductor Device Advances

• Finer device features:
  from submicron (0.1 – 0.5 µm) to nanometer (10 – 100 nm)

• Higher I/O count:
  from 100’s of I/O to 1000’s of I/O

• Lower Operating Voltage:
  from 1.5 – 2.5 V to less than 1V

• Increased Power Density:
  from 1 – 10 W/cm² to 20 – 50 W/cm²

• Faster Clock Rates:
  from 1 – 3 GHz to 3 – 10 GHz
These Semiconductor Trends are having significant impact on every aspect of electronic packaging and interconnection

- **Increasing chip I/O count driving package I/O’s.**
  - perimeter I/O to area array I/O
  - tighter package I/O pitch
  - finer substrate/board interconnect density

- **Increasing chip clock rates driving interconnect.**
  - finer line pitch
  - lower dielectric constant
  - lower dielectric losses

- **Increasing power dissipation driving package designs.**
  - improved interface materials
  - more complex cooling structures
ITRS Roadmap Defines Six Main Market Segments

- **Low-cost:** <$300 consumer products, microcontrollers, disk drives, displays
- **Hand-held:** <$1,000 battery-powered products, mobile products, hand-held cellular telecommunications, other hand-held products
- **Cost-performance:** <$3,000 notebooks, desktop personal computers, telecommunications
- **High-performance:** >$3,000 high-end workstations, servers, avionics, supercomputers (the most demanding requirements)
- **Harsh:** Under-the-hood and other hostile environments
- **Memory:** DRAMs, SRAMs
Two of These Electronics Market Segments are the Key Driving Forces Behind Today’s Advanced Packaging and Interconnection Technology Advancements:

• **Hand-held**: <$1,000 battery-powered products
  • small size, mixed technologies, moderate performance
  • highest volume, most cost driven

• **Cost-performance**: <$3,000 computing
  • driving high power, high I/O, high speed
  • large volumes, moderate cost factors
There are four basic elements that define the structure of a microelectronics package:

• The electrical connection of the chip to the package
  • wirebond, solder bump, TAB, adhesives, other

• Encapsulation of the chip
  • underfill, overmold, injection or transfer molding

• The structure of the package
  • ceramic, organic substrates, metal
  • molded leadframe

• The connections of the package to the circuit board
  • thru-hole, leaded, leadless, array pads, BGA, etc.
We will next look at the basic elements of various microelectronics packages as they evolved over the past few decades with the evolution of the semiconductor device industry.
Standard PTH Electronics Packages (60’s-70’s)

Dual-in-Line Plated-Through-Hole Packages

- **Plus:**
  - Robust lead-in-hole attach
  - Low cost package

- **Negative:**
  - Limited to 100 mil pitch
  - Limited to about 64 I/Os
  - Limited PCB density

Source: KTH
Leaded SMT Carrier Evolution (70’s – 80’s)

Surface Mount Perimeter Ledged Packages

• Plus:  
  - tighter lead pitch to 25 mil pitch
  - higher I/O count to >200
  - allowed increased PWB density
  - lead compliance

• Negative:  
  - assembly yield; shorts/opens
  - more costly package

Source: KTH
Leaded Carrier Evolution

Schematic of a Plastic Quad Flet Pack (PQFP) with:

- the silicon chip
- the lead frame
- wire bonds
- molding compound
- die attach adhesive
- die attach paddle

Source: KTH
Perimeter I/O Package Limitations

As the high-end semiconductor device I/O count kept increasing to >250, the perimeter leaded carrier ran into physical limits in its lead pitch and package size.

Let’s look at how the perimeter package is effected with increasing I/O count.
Perimeter I/O Package Size vs. I/O
We fix lead pitch at 1.2 mm (50mil)

Fixing lead pitch drives package size up, severely

And not shown because of size!
96 I/O Leaded FP (4x)
Package Area = 1024 mm² (16x)
**Leaded Package I/O and Size Limits**

We fix package size at 64 mm² (8 mm x 8 mm)

- **24 I/O**
  - Leaded FP
  - @ 1.20 mm pitch
  - Die

- **48 I/O**
  - Leaded FP
  - (2x)
  - @ 0.60 mm pitch
  - Die

- **96 I/O**
  - Leaded FP
  - (4x)
  - @ 0.30 mm pitch
  - Die

Fixing package size drives lead pitches down severely, to point that they are too costly, have assembly yield and have poor reliable.
Leaded Package I/O and Size Limits

As I/O counts continued to increase by factors of 2X to 4X every year or two, perimeter I/O packages become a less viable option:

- very expensive
- excessive size
- poor assembly yields
- poor reliable
A Broad Spectrum of New Packaging Approaches Were Developed to Overcome Perimeter Package Limitations:

- Advanced BGA Carriers
- Flip Chip in Carrier & Flip Chip on Board
- Chip Scale Packages
- Multichip Modules, System-in-a-Package (SIP)
- 3-D Assemblies
- Integral Passives
- Integrated, Point-of-Load Power Conversion
- High Density Interconnect Substrates
- Optical Interconnect
Area Array Package I/O and Size Capabilities

We fix pad pitch at 1.2 mm (50mil)

25 Pad Array Package
@ 1.20 mm pitch
Package Area = 50 mm²

100 Pad Array Package (4x)
@ 1.20 mm pitch
Package Area = 200 mm² (4X)

Fixing pad pitch permits a 4x increase in I/O for a 4x increase in package size!
Area Array Package I/O and Size Capabilities

We fix package size at 49 mm$^2$ (7 mm x 7 mm)

25 Pad Array Package
@ 1.20 mm pitch
Package Area = 49 mm$^2$

100 Pad Array Package (4x)
@ 0.60 mm pitch
Package Area = 49 mm$^2$
4X I/O Count => ½ pad pitch

Fixing package size permits a 4x increase in I/O for only a 2x decrease in pad pitch
Perimeter vs. Area Array Package Pitch

With a fixed package size, increasing I/O count by 4x requires:
a 4x decrease in perimeter pad pitch!
or a 2x decrease for array pad pitches

96 I/O Leaded FP (4x)
@ 0.30 mm pitch
Package Area = 64 mm²
4X I/O Count => ¼ I/O pad pitch

100 Pad Array Package (4x)
@ 0.60 mm pitch
Package Area = 49 mm²
4X I/O Count => ½ pad pitch
Perimeter vs. Area Array Package Size

With a fixed I/O pitch, increasing I/O count by 4x requires:
- a 16x increase in perimeter package size!
- or a 4x increase for array package size!

96 I/O Leaded FP (4x)
Fixed 1.2 mm lead pitch
Package Area = 1024 mm² (16x
32 mm X 32 mm)

100 Pad Array Package (4x)
Fixed 1.20 mm pad pitch
Package Area = 169 mm² (<4X)
13 mm X 13 mm
So high-end semiconductor devices I/O count from 256 and up require semiconductor device packages with area array I/O pads.

We will now look at how different market segments drove the next generation package and assembly technologies.
Let’s Look at the High End Cost-Performance Microelectronics Market Segment

Product Lines

• Desk Top PC’s
• Workstations
• Low-End Servers

Packaging Needs

• Very High I/O Count
• High Power Dissipation
• Lower Supply Voltage
• High Clock Rates
• CTE Stress Issues

These Cost-Performance Systems Rode the Leading Edge of the Semiconductor Performance Wave in Terms of I/O Count, Power Dissipation, Operating Voltage, and Clock Rate.
Advanced Packaging Approaches
Developed for Cost-Performance Systems

• Wire Bonded Chips in BGA Carriers
• Flip Chips in PGA and BGA Carriers
• Molded BGA Packages
• Multichip Modules
• 3-D Stacked Modules

Cost-Performance Systems migrated to area array packages, avoiding chip on board approaches due to device costs, power, I/O pitch and repairability issues.
What is the Function of a High-End Microelectronics Package?

- Environment & mechanical protection:
  - moisture, fluids, shock, etc.
- Electrical connections: chip to the board:
  - from microns to millimeters.
- Stress isolation: chip from the circuit board:
  - low CTE silicon and high CTE polymers.
- Efficient heat removal:
  - direct thermal path, chip to ambient
Mid-Range I/O Packages: 100 – 300 I/O

Motorola’s Molded Array Process PBGA

Wire Bonded Chip on Organic Substrate with Molded Cap Capable of Several Hundred I/O.

Source: Motorola
Mid-Range I/O Packages: 300 – 500 I/O

TI (TBGAII) Tape Ball Grid Array Package

- a single tier, single layer package targeted at ASICs & DSPs
- die is mounted on a copper heat spreader for 5 watt chips
- tight staggered wire-bonding supports high-frequency
- level 3 moisture sensitivity.

Source: TI
Mid-Range I/O Packages: 300 – 500 I/O

**Fujitsu Face Down Heat-Spreader BGA**

- dual copper leadframe/heat spreader.
- uses transfer molding.
- has 2 to 4 layers of high Tg FR-4.
- low profile, less than 1.4 mm.
- reduces weight.
- meets JEDEC MSL-3.

![Fujitsu Face Down Heat-Spreader BGA](image)

Source: Fujitsu
Mid-Range I/O Packages: 300 – 500 I/O

0.4 mm pitch
288 pins
10 mm/side
35 µm lines/spaces
90 µm via hole dia.
two metal layers

Source: NEC
IBM’s Organic BGA Carrier Built by Endicott Interconnect

Built using the Surface Laminar Circuit with micro vias and thin Cu, exceeding 1,000 BGA I/O pads. Chips are attached by fine gold wirebonds with bond pad pitch spacing as low as 60 microns or less.
High-end-Range I/O Packages: 500 – 1000 I/O

Fujitsu Tape Ball Grid Array Package
With Cu Heat Spreader

Source: Fujitsu
Flip Chip Device Technology

The move to area array chip connections, primarily flip chip solder bumps, from perimeter wire bonds was driven by the same forces that drove packages from perimeter to area array connections:

- Increasing I/O counts.
- Increasing clock rates.

And;

- package cost.
- component reliability.
Flip Chip Device Technology

Wirebonds were generally restricted to the chip perimeter, and a 2x increase in I/O count requires either:

• cutting wirebond pitch in half, causing yield issues
  or
• increasing in chip size by 4x, increasing chip cost

Wirebonds have significant resistive and inductive losses:

• limiting switching frequencies & device clock rates.
  and
• increasing EMI radiation & switching noise.

These are the same limitation seen on leaded carriers
Flip Chip Device Technology

- Wirebonds are the number one device reliability issue due to the creation of microcracks in the chip or its overglass passivation, and to the CTE mismatch inherent with the bond structure.

- Area array flip chip solder bumps and other array attach technologies, open the entire chip surface to bond pads and created the flip chip.
  - permitting many more I/O on a larger pitch on the same chip size
  - eliminating more than 90% of the interconnect parasitics.
Flip Chip Device Technology

IBM is generally credited with the development of Flip Chip attach when in the early 1960’s they developed their Controlled Collapse Chip Connection (C-4) process.

• The first C4 process in the 1960’s, used Cu spheres with solder paste attach, for few I/O only.

• As I/O counts increased, IBM moved to a high temperature solder bump (97/3\% Pb:Sn) that reflowed during attach (~300 °C).

• This was used on a low CTE (6-9 ppm/°C) ceramic substrate that could handle the high reflow temperature and had low CTE stress on the solder joints.
Flip Chip in a Package

When other companies looked at using flip chip, they needed a simpler, lower cost structure than the complex IBM flip chip on co-fired ceramic MLB.

They developed a flip chip in ceramic package approach:

• flip chip devices are mounted in ceramic chip carriers using either the IBM C-4 process under a license from IBM or using an all eutectic solder ball process.

• the ceramic carrier provided a good CTE match for the flip chip devices, thus avoiding solder fatigue failures.

• the carrier was then solder onto a organic MLB with large pitch pads or leads.
Flip Chip in a Package

- The flip chip in ceramic carriers then had either leaded I/O for board attach or area array I/O.
  - flip chip pitch: 0.250 – 0.350 mm
  - leaded carriers had I/O pitches of 0.4 to 1.0 mm
  - array carriers had I/O pitches of 1.27 to 1.5 mm
Flip Chip Device Technology

As other companies put the C4 process into production, they first used the high lead solder process on ceramic carriers. When they moved to organic substrates for lower costs, the process was modified:

• New C-4 uses a high temperature solder bumps (97/3% Pb:Sn) with eutectic Pb:Sn solder paste was used to solder the high temperature solder ball to the substrate at 218°C.

• The C-4 solder ball does not reflow during solder attach, maintaining a higher bump height.

• The low temperature solder attach minimized stress caused by the high CTE organic board on the solder joints.
C4 Flip Chip Device Technology

C4: Controlled Collapse Chip Connection Solder Joints On Organic Carriers

Source: IBM
Eutectic Flip Chip Technology

Unlike C4 Solder Joints, Eutectic Solder Joints Collapse by 30-50% During Reflow Provide Less Joint Compliance
Eutectic Flip Chip Technology

Eutectic Sn:Pb Solder Ball

Source: Fraunhofer IZM

Source: Flip Chip Technologies
Flip Chip Limitations

But, flip chip devices could not easily be used in lower cost organic carriers, nor mounted directly onto organic substrates because of the high CTE of organic materials.

Source: Circuits Assembly
Flip Chip Limitations

Because of the scarcity of flip chip devices and the issues of solder fatigue on organic substrates, use of flip chip technology has been limited to:

- large vertically integrated companies
  - IBM, Motorola, Fujitsu, etc.
- high end semiconductor devices (microprocessors)
- high end computer systems (servers, work stations)

As chip sizes increased and high CTE organic carriers were used, flip chip solder fatigue became a limiting issue.
Flip Chip Underfill is Born

• Tradition has it that when IBM was looking at replacing C-4 bumps with indium solder that could be used to form connections without high temperature they became concerned with moisture causing electro-migration.

• In order to prevent moisture from getting to the joints, they sealed the solder joints with an underfill composed of an organic material such as an epoxy or silicone.

• They found that amide-imide underfilled joints extended fatigue life up to 10x that of solder joints without underfill!
Flip Chip Underfill

• When applied to a flip chip device, underfill encapsulates the area between the active side of a flip chip and the substrate upon which it is mounted.

• The underfill material protects the interconnect area from moisture and other environmental elements, and it reinforces the mechanical connection between the substrate and the die.

• Once cured, the underfill material provides additional mechanical support to the solder joints, protecting them from cracking and failing.
**Flip Chip Underfill - Reliability**

Low Reliability without Underfill if: Low CTE Chip Mounted onto High CTE Substrate

High Reliability with Underfill if: Low CTE, High Tg Underfill

Silicon Die – CTE = 3 ppm/C

Plastic Substrate – CTE = 17 ppm/C
Flip Chip Underfill

• The process of underfilling a flip chip typically involves capillary action and often is considered to be a production bottleneck.

• Underfill requires equipment, floor space and extended time in curing ovens, and thus adds costs.

• These production issues have lead to development efforts in both Wafer Level Underfill and No-Flow Underfill (covered later in this presentation).
Flip Chip in Organic Packages

We will look at some examples of leading edge microprocessors that are flip chip assembled in organic chip carriers by either the vertically integrated semiconductor manufacturers, by contract assemblers or in packaging research institutions.
ASE Flip Chip BGA

- Four layer laminate, 4~8 layer build-up, and ceramic substrates are available for different application
- Experience of max die size 18 x 18 mm²
- Chip capacitor attach is available
Flip Chip on Thin film Interposer Technology

Chip Down

Chip Up

Thin film organic laminate substrate
Redistribution from flip chip to BGA

60 μm perimeter bump pitch flip chip

Source: IMEC
Flip Chip in a Package

Amkor Flip Chip BGA

Substrate features:
- a two layer organic core
- three built-up layers per side
- micro-vias
- chip underfill
- four decoupling capacitors

Source: Amkor
Fujitsu Flip Chip Organic Carrier with Copper Alloy Lid/Thermal Spreader

High I/O Count Flip Chip Devices Stress the Interconnect Capability of the Chip Carrier Interposer/Substrate

Source: Fujitsu
IBM Microprocessor Area
Array Chip Carriers

Ceramic & Plastic
Thermal Enhancements
Wire Bond & Flip Chip
Solder Ball
Solder Column
Low I/O Count: 100’s
High I/O Counts: 1000’s

Source: IBM
Intel 90nm, Low K Microprocessor in an Organic Flip Chip Ball Grid Array Carrier

Interposer Lines 1/3 the Size of a Human Hair
Intel Pentium4® PGA Package
Flip Chip Carrier

Center Core PCB with Build-Up Redistribution Layers (3:2:3)

Source: Intel
IBM’s (EI’s) High Performance Chip Carrier (HPCC)

- Flip Chip on Laminate
- Low Electrical Parasitics
- High Speed Capabilities
- Capillary Underfill
- Controlled Transmission Lines
- Low Power Distortion
High Density Organic Chip Carrier Substrates
Complexity, Cost Increase with I/O Count

**Thick Core Organic Substrate**
**4-4-4 Build-Up Center Core**
- Center Core with Drilled Thru-Holes
- Four Topside Micro-Via Layers
- Four Bottom Side Micro-Via Layers

**Thin Core Organic Substrate**
**3-2-3 Build-Up Thin Core**
- Thin Center Core with Laser Micro-Vias
- Three Topside Thin, Micro-Via Layers
- Three Bottom Side Micro-Via Layers
- Lower Cost, Thinner Substrate

Source: Fujitsu
GE’s Chips First Build-Up™
µP Package
High-End Grid Array Carriers

Although most high-end grid array carriers utilize Ball Grid Array (BGA) solder connections to the circuit board there are the option for Column Grid Array (CGA) Land Grid Array (LGA)
Column Grid Array (CGA) is an alternative to Ball Grid Array (BGA) in area array packages.

Source: Advanced Packaging
- Increased physical compliance during mechanical stress conditions such as from thermal cycling or warpage.

- Column Grid Array Packages can survive wider temperature excursions and increased number of thermal cycles.

Source: Advanced Packaging
Pin Grid Array (PGA)

- Has a pin soldered to array pads using high temp solder
- Permits the use of sockets to simplify processor change-out
- Survives increased number of thermal cycles.

Source: Digital Life
Pin Grid Array (PGA)

SUN UltraSPARC Iii PGA Processor 650 MHz

AMD Athlon PM 2100+ PGA with topside passives 1.73GHz, 130nm technology

Source: Digital Life
Pin Grid Array (PGA)

VIA Technologies C3
1.0 GHz, 130nm technology

Intel 1.9 GHz Pentium 4
PGA with passives

Source: Digital Life
Flip Chip Market Share

Even with all of the density and performance advantages that Flip Chip has, it is a small but rapidly growing market segment of the Semiconductor device market:

• In 2000, Flip Chip accounted for only 2% of all ICs shipped, 1.8 billion out of 86 billion.

• In 2002, Flip Chip grew to 3.3% of all ICs shipped, 2.6 billion out of 79 billion.

• By 2007, Flip Chip is forecast to grow to 8% of all ICs shipped, 9.1 billion out of 114 billion.

• From 2002 to 2007, Flip Chip is forecast to have a 28% Compound Average Annual Growth Rate (CAAGR) as opposed to the overall IC market CAAGR of 7.7%.

Source: Prismark

Flip Chip is becoming the dominant interconnect technology of for high I/O count, high speed ICs
Multichip Technologies

Another advanced packaging approach that has been developed to support the electrical performance requirements of the Cost-Performance Market is Multichip.

As opposed to single chip packaging where one IC is placed within a package, multichip packaging puts two or more ICs into a common package or module. These include:

- Multichip Modules (MCM), many chips
- Multichip Packages (MCP), few chips
- System-in-a-Package (SiP)
- System-on-a-Package (SOP)
Multichip Technologies

• In the 1980’s, Multichip Modules were originally developed for aerospace applications, where size and weight were critical requirements and there 10’s of ICs in the same package.

• Recently, Cost-Performance applications turned to few chip, Multichip Packages with two to six ICs to achieve faster processor to memory data rates and lower board level I/O.

• Multichip Packages were also developed to put more memory into a limited board area.
Multichip Module Technologies

KTH Digital MCM

Six Chip, Flip Chip on Polymer MCM

Source: FlipChip Dot Com

Thin Film Digital MCM

Si Substrate MCM

Fetal Monitor

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Multichip Module Technologies

Mixed Analog/RF/Digital MCMs

Source: Royal Institute of Technology (KTH)
Multichip Module Technologies

Typical Few Chip MCPs with Flip Chip or Wire Bonded Devices on Organic Substrates

IBM Few Chip Multichip Modules
Multichip Module Technologies

Direct chip attach of bare die on laminate board. Limited to low I/O count by PCB capabilities

Source: IMEC
Multichip Module Technologies

RF Monolithics ASH Multichip Module

Source: Prismark/Binghamton University
Wire Bonded Chips onto Polymer Substrate with BGA Connections to Board

Source: Amkor

Philips MCM/BGA for Consumer Product
System-in-a-Package (SiP)

A version of multichip technology that generally a combination of digital, analog, power and/or RF onto a low cost substrate.

SiP offers key advantages of handheld wireless products by concentrating the RF portions of a circuit into a manageable unit.

- reduces the performance requirements and cost of the PCB
- minimizes the size, complexity and cost of EMI shielding
- more readily incorporates high precision integral passives
- minimizes system parts count
Multichip Module Technologies

System-in-a-Package (SiP)
Wirebonded Chips on Organic Substrate with Plastic Encapsulation and Solder Ball Attach

Source: ASAT
Multichip Module Technologies

System-on-a-Package (SOP)

Source: Georgia Tech
Multichip Module Technologies

GE Global Research Developed Multichip Module Technologies:

Embedded Chip-on-Flex (COF)
1. Single sided vendor flex.

2. Apply die attach adhesive

3. Attach die.

4. Mold.

5. Drill-1, metal-1

6. Lamination-1, drill-2, metal-2

7. Attach & Reflow Solder Balls.

Chip-on-Flex Process Flow:

Featuring: Polyimide Film Dielectric Layers, Laser Microvias, Ti:Cu Sputter/Electro-Plate Metallization, Plastic Encapsulation
Chip-on-Flex Multichip Cross-Section
GE Global Research Chip-on-Flex Technology

100W Point of Load Power Converter

GPS Mixed Mode Module

200V/150A Power Switch

Thinned Cellular Phone Module

Mixed Mode with Integral Passives
In Summary, Cost-Performance Systems Have Driven Packaging Technology to:

• Move packages from leaded to area array to reduce package sizes and support faster clock rates.

• Move Flip Chips into the mainstream to handle very high I/O counts and faster clock rates.

• Use Fine Line Interposers to fan-out from the chip pitch to the PCB pitch and to mechanically isolate the chip CTE from that of the PCB.

• Go to Multichip Packages to move chip clusters closer together to save area and to support higher frequency operation.
Advanced Packaging Technology for Leading Edge Microelectronics and Flexible Electronics
Part 2

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Let’s now look at the
Portable Electronics Market Segment
And Its Effect on Advanced Packaging
Portable Electronics Market Segment

Product Lines
• Cellular Phones
• Pagers
• PDAs
• Digital Cameras
• Memory Cards
• Smart Cards
• Security Cards
• Medical Monitors
• Lap Top PCs

Segment Characteristics
• High Volumes
• Being Fast to Market
• Short Product Life

Critical Requirements
• Cost, Cost, Cost!
• Small Size & Light Weight
• Thin Profiles
• Low Power, Low Voltage
• Mixed Analog, RF, & Digital
• EMI Specifications
Portable Electronics Market Segment

Driven by the need to add more functionality, features and components at a lower cost, into a shrinking product envelope.

Driving advanced packaging technologies such as:

- Low Cost, non-Flip Chip, Array Attach
- Chip-on-Board, Chip Scale Packages
- Mixed Digital, Analog and RF MCPs (not MCMs)
- 3-D Chip Packages
- HDI PCBs with Fine Lines and Microvias,
- Fine Line Flex with Integral Passives
Portable Electronics Products

Cell Phone with EMI Shielding
Cell Phone Circuit Card
Cell Phone Circuit Card with Metallized Plastic Enclosures

Cell Phones Driven by Size, Features, Cost.

Source: Prismark

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Portable Electronics Products

Portable Products from IC Recorders to Internet Wireless
Put Ever More Functionality into Ever Smaller Hardware.

Source: Prismark

Panasonic IC Recorder  Intel Wireless LAN Card

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Portable Electronics Products

Casio Wrist Camera WQV-1-8JR

Casio Wrist Camera with Chip Scale Package.

Source: Fujitsu
Portable Electronics Products

Hybrid Cellular Phone from Sanyo with Fujitsu Chip Scale
Portable Electronics Products

Portable Electronic Manufacturers Are Turning to Small Footprint Packages Like These Chip Scale Packages.
Low Cost Flip Chip for Chip on Board and Low Cost Packages

For Portable Electronics
Non-Solder Bump Flip Chip Attach

Alternative array attach processes have been developed to replace solder bump attach, targeting lead-free, higher pad pitch, reduced assembly temperature, increased compliance and most importantly, lower cost.

- Adhesive Bonding:
  - Conductive Adhesives:
  - Anisotropic Conductive Adhesive:
  - Non-Conductive Adhesives:
- Metal-to-Metal Bonding:
- Direct Metallurgical Contacts:
Flip Chip Adhesive Bonding Process Options

• **Isotropic-Conductive-Adhesive (ICA):**
  • Adhesive equally conductive in all directions
  • Plated Au Pads, Au Bond Bumps

• **Anisotropic-Conductive Adhesive (ACA):**
  • Adhesive conductive in one preferred direction
  • Plated Au Pads, Au Bond Pads

• **Anisotropic-Conductive Film (ACF):**
  • Metal coated polymer spheres in a film adhesive
  • Plated Au Pads

• **Non-Conductive Adhesive (NCA):**
  • Adhesive not conductive in any direction
  • Au Stud, Ni/Au Pads, Nano-Pierce Au
Isotropically Conductive Adhesives (ICA) are polymer adhesives filled (typically) with small silver flakes that are electrically conductive conduct equally well in all directions.

The bonding process uses screen printing or dipping the conductive adhesive onto the Au plated array bumps.

Curing is done at a lower temperature than conventional solder reflow.

Since cleaning is no longer needed, the underfill process, which is required, can begin immediately.
Flip Chip Adhesive Attachment Processes

- Ni-Au bump after dipping in conductive adhesive.
- The rounded-corner "loaf" shape is typical of electroless plated bumps.
- Conductive silver particles in the adhesive can be seen coating the bonding surface.
SEM cross-section of a Ni-Au bump assembled with stenciled conductive adhesive. The conductive adhesive forms a fillet of fine-grained silver particles around the bonding surface, while the underfill adhesive fills the remaining space.
Stud-Bumping ICA Assembly Process

application of adhesive by dipping

alignment

placement
**Isotropically-Conductive Adhesive (ICA)**

- **Au Stud Bump on Chip Pad**  
  ~ 75 microns diameter  
  Does not require UBM

- **Au Stud Bump Bonded to Substrate Pad Using Conductive Adhesive**  
  ~ 25 microns Bump Height
Flip Chip Adhesive Attachment Processes

- ACAs contain conductive particles such as nickel or gold balls or nickel or gold-coated polymer balls.
- Contact pads on the chip and the substrate are gold plated.
- The adhesive shrinks during curing and the conductive balls form an electrical connection from the component pad to the substrate pad.
- And since the adhesive is used over the entire surface, no underfill is required—which eliminates an entire process step.
Anisotropically Conductive Film Attach Process

- During the bonding process, the insulation in the Z-axis between pads is pushed away.
- The Ni-Au layer on the particle makes electrical contact between the IC and the substrate, while not shorting in the X and Y directions.
- The epoxy cures, locking the particles in this compressed state.
- The elasticity of the compressed trapped particles causes them to constantly press outward on both contact points.
- This helps maintain electrical connections through a wide range of environmental conditions.

Source: SONY Chemical Company
Non-Conductive Adhesive (NCA)

- Another option for adhesive flip-chip joining is the use of a non-conductive adhesive applied to the whole surface before the chip is positioned.
- The interconnect is established when heat and force are applied to the die during the bonding process.
- The adhesive shrinks upon curing, pressing the bumps more tightly against the pads and forming the conductive contact.
- The underfill process is not required, potential cost reduction.
- Does not require UBM on chip pads.
Thermo-Compression/Thermo-Sonic Microwelding
Au Stud to Au Pad Flip Chip Device Technology

• Au Stud Formed on Chip Pad

• Bonding Process: Heat, Pressure, Sonic (optional)

• Au Stud Microwelded to Substrate Pad

• Au Stud Bump Tip is Flattened During Bonding Process

• Does Not Require UBM on Chip Pads
Thermo-Compression or Thermo-Sonic Microwelding
Au Stud to Al Pad Flip Chip Device Technology

Source: Flip Chip DOT COM
Direct Metallurgical Contact: Polymer on Chip

- Bare Chips mounted face down onto plate and back side encapsulated
- Plate Removed and top surface coated with polymer dielectric
- Vias formed over chip pads by photodefinition
- Sputter/electroplate processes used to electrically connect chip pads to flex interconnect

Example: Intel BBU

![Image showing on-chip interconnect, chip bond pad, build-up layers, and pre-solder for attach with red arrows pointing to each feature.]

Source: Intel
Direct Metallurgical Contact: Chip on Film

- Bare Chip Bonded to Flex with adhesive
- Vias formed over chip pads
  - laser ablation
  - plasma, RIE etch
- Sputter/electroplate processes used to electrically connect chip pads to flex interconnect

Example: GE Chip-on-Flex (COF)

Source: GE
Chip Scale Packaging
10% to 100% Larger Than the Chip

Near Flip Chip Densities without Flip Chips

Packaged Part Robustness without the Size Penalties of a Packaged Part

Standard Pad Configuration, Multi-Sourcing

The Ultimate in Small Packages
Chip Scale Packaging

Comparison of the footprint requirements of a Leaded QFP, a Flex BGA and a Wafer Level CSP

Key Driving Forces Behind CSP Devices are:
Footprint Area Reduction, Package Thickness Reduction and High Electrical Performance

Source: OKI

<table>
<thead>
<tr>
<th>Chip Size 8 x 8 mm</th>
<th>144 Pin LQFP</th>
<th>144 Pin FBGA</th>
<th>144 Pin W-CSP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin Pitch</td>
<td>0.5 mm</td>
<td>0.8 mm</td>
<td>0.5 mm</td>
</tr>
<tr>
<td>Package Size</td>
<td>20 x 20 mm</td>
<td>13 x 13 mm</td>
<td>8 x 8 mm</td>
</tr>
<tr>
<td>Mounting Area</td>
<td>484 mm²</td>
<td>169 mm²</td>
<td>64 mm²</td>
</tr>
<tr>
<td>Package Weight</td>
<td>1.4 g</td>
<td>0.3 g</td>
<td>0.08 g</td>
</tr>
</tbody>
</table>

MSE 542 Ray Fillion, GE Global Research - Slide 26
Renesas Land Grid Array Package
Small, Thin Packages for Portable Electronics

- smaller size with area array pads
- thinner packages by eliminating solder balls and using thinned chips
Wire Bonded Grid Array Chip Carriers

Optical chip scale carriers for camera sensors and BGAs for memory chips can be built on the same sized substrate strips.

DRAM chips are assembled nine-up for each index at wire bonding on this chip-scale BGA substrate strip.

Source: Kingpin Technologies
ASE Very Fine Pitch BGA (VFBGA)

VFBGA is commonly used in cellular phones, hard disk drives, PLD’s, digital camera and many others that demand thin packages. This package is often used for SRAM, Flash, EEPROM, ASIC, PLD & analog products.
Chip Scale Packaging Thickness Trends

Chip Scale Packages Are Driving to Thinner and Thinner Profiles (0.35 mm)

Source: Prismark
Chip Scale Packages Are Driving to Smaller and Smaller Ball Sizes (0.21 mm) and to Tighter and Tighter Ball Pitch (0.35 mm).

Source: Prismark
Wafer Level Chip Scale Packaging

Integrating Chip Scale Packaging into the Wafer Fabrication Back-end
**Wafer Level Chip Scale Packaging**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
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<tr>
<td>Analog</td>
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<td>38</td>
<td>59</td>
<td>115</td>
<td>238</td>
<td>496</td>
<td>874</td>
<td>975</td>
<td>75.5%</td>
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<tr>
<td>Standard logic</td>
<td>15</td>
<td>26</td>
<td>44</td>
<td>81</td>
<td>217</td>
<td>356</td>
<td>459</td>
<td>475</td>
<td>61.2%</td>
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<tr>
<td>MCU</td>
<td>19</td>
<td>31</td>
<td>43</td>
<td>75</td>
<td>212</td>
<td>421</td>
<td>539</td>
<td>606</td>
<td>69.4%</td>
</tr>
<tr>
<td>Image sensor</td>
<td>2</td>
<td>4</td>
<td>5</td>
<td>12</td>
<td>26</td>
<td>39</td>
<td>64</td>
<td>76</td>
<td>69.2%</td>
</tr>
<tr>
<td>Memory</td>
<td>12</td>
<td>20</td>
<td>35</td>
<td>54</td>
<td>118</td>
<td>249</td>
<td>400</td>
<td>472</td>
<td>68.3%</td>
</tr>
<tr>
<td>Passive</td>
<td>106</td>
<td>212</td>
<td>425</td>
<td>850</td>
<td>1700</td>
<td>3675</td>
<td>4280</td>
<td>5470</td>
<td>66.7%</td>
</tr>
<tr>
<td>Others</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>9</td>
<td>14</td>
<td>19</td>
<td>18</td>
<td>45.3%</td>
</tr>
<tr>
<td>Total</td>
<td>186</td>
<td>332</td>
<td>614</td>
<td>1190</td>
<td>2520</td>
<td>5250</td>
<td>6635</td>
<td>8092</td>
<td>67.5%</td>
</tr>
</tbody>
</table>

*Source: Gartner Dataquest

Gartner Dataquest has very high WLCSP unit forecast in 2007;
- total units at 8092 MM;
- with memory at 472 MM, and ACIC, Logic & MCU at 606 MM
Typical Wafer Level CSP Process Flow

**Wafer from Fab**

1. **Incoming Wafer**
2. **Cu/TiW Seed Layer Deposition**
3. **Spin on Photoresist**
4. **Expose and Develop Photoresist**
5. **Plate Copper Inductor and Stud**

**Etch Cu and TiW seed layers**

**Deposit BCB and Pattern for Bump**

**Place and Reflow Solder Ball**

Source: Amkor
Wafer Level Chip Scale Packaging

Wafer Level CSP Technologies Minimize Die Handling by Forming the Device Package as a Backend Wafer Processing Step and Target Minimizing Packaging Costs

Source: OKI
Wafer Level Chip Scale Packaging

Wafer Level CSP Technologies Redistribute the Tight Pitched, Perimeter Chip Wirebond Pads to a Larger Grid Area Array Configuration Compatible with Solder Ball Attach
**Wafer Level Chip Scale Packages**

**Typical Wafer Level CSP Configurations**

Source: OKI
Unitive Wafer Level CSP Pad Redistribution

Source: Unitive

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Center Pad SDRAM CSP
Source: Micron

Typical WL-CSP Devices

Source: Amkor

Source: Micron

Source: Unitive

Source: Prismark

Source: IMEC

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Wafer Level CSP & Other CSP
Solder Bump and Underfill Processes

Area Array Solder Bumps are used to form electrical connections to the next packaging level, the PCB.

• Key aspects of this process are:
  • bump formation process
  • under bump metallization process
  • compliant under bump structures

We will now take a look at these areas:
**Solder Bump Flow**

- Sputtered Seed Layers
- Resist Coat
- Plate Solder
- Strip Resist
- Expose and Develop
- Plate Ni Barrier Layer
- Reflow Solder
- Seed Layer Etch

Source: Unitive
CSP Solder Bump Formation

Paste Dispense, Ball Placement and Reflow Solder Ball Formation

Electroplated and Reflowed Solder Ball Formation

Solder Paste Dispense and Reflow Solder Ball Formation

Source: Fujitsu

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Solder Sphere-Jet Bumping
350 micron jetted bumps on a CSP strip

- Laser heating to reflow the ball before it reaches the substrate.
- Sphere becomes a molten solder jet before contacting the pad.
- High speed, flux free non-contact placement and reflow
- Rates up to 10 balls per second
- Diameters may be from 100 to 760 micrometers.

Solder Sphere Ink Jetting Bumps

Source: PacTech
Wafer Level Chip Scale Packaging

A Major Issue Facing CSPs is the CTE Induced Solder Fatigue and Underfill is a Costly Solution When Applied to a CSP on a PCB.

A Wide Variety of Stress Relieving Structures Has Been Developed to Mitigate the Fatigue
K & S Polymer Layer Wafer Level CSP

Bump on Nitride (BON) Cross-Section

Bump on Polymer (BOP) Cross-Section

Solder
PI 2 Layer
UBM & RDL
PI 1 Layer
Wafer

Solder
UBM Layer
PI 2 Layer
RDL Layer
PI 1 Layer
Wafer

Spheron BOP WL CSP
K & S Flip Chip Technologies
Polymer Collar Wafer Level CSP
Targeting a 50% Increase in Fatigue Life

Source: K&S-FCD
IMEC, Belgium, Elastomeric Under Pad Bump
Targeting a 100% Increase in Fatigue Life

Source: IMEC
Casio, Fujitsu & Oki WLCSP With Cu Posts

Targeting:
• Increased Compliance
• Reduced Solder Fatigue
• 100% Increase in Life
Fraunhofer IZM Double-Ball Solder Attach Wafer Level CSP

Approaching a Solder Column Structure Providing Increased Solder Height Increased Compliance

Source: Fraunhofer IZM
Tessera Single Chip MicroBGA® Packages

Elastomeric Structure Over Die Surface Provides Significant Mechanical Compliance, Avoiding CTE Induced Solder Fatigue Without Underfill
COF Chip Scale Process Converts Perimeter I/O Die into Standard Area Array Solder Ball Packages
GE Floating Pads Technology: Stress-Free Solder Attach
Three-D and Stacked Chips

3-D Driving Forces:
- More Memory Located Close to µP
- Faster Operation
- Mixed Memory, Processor and Analog ICs
- More Functionality in Same Footprint
- Lower EMI, Less EMS

Issues
- Thermal Dissipation?
- Cost?
- Yield?
- Need for Thinned Die
3-D Stacked Modules Driving Need for Thinned Die, Thinned Wafers

- 100 microns baseline for thinned wafers
- 50 microns current developmental
- 25 microns demonstrated.
- major issues with wafer handling, die handling, die bonding and die wire bonding

Source: Fujitsu
Intel Ultra-Thin Stacked Chip Carrier Packages

- 4-5 Die Stack
- Die Thinned to 75 µm
- 1-1.2 mm Height
- Wire Bonded

Source: Intel
Intel Ultra-Thin Stacked Chip Carrier Packages
Wire Bonds vs Thru Wafer Vias

- Spacers utilized for wb between same size die
- Eliminated with through silicon via interconnect

Source: Intel
Fujitsu Stacked Multichip Packages

3-Chip Stacked, Wire Bonding

3-Chip Flip Chip & Wire Bonding

Source: Fujitsu
Fujitsu Stacked MCP

8 Chip Stack

5 Chip Stack

Stack Configuration

SEM Cross-Section

Source: Fujitsu
Fujitsu Wafer Level Stacked MCP

No Process Information Yet Available on the Fujitsu Wafer Level Stacked MCP. Similar to Fraunhofer IZM Structure and GE Chip on Flex Structure

Source: Fujitsu
ChipPAC Stacked SiP I
Wire Bonded Die-Up

Source: ChipPAC

ChipPAC Stacked SiP II
Wire Bonded, Die-Up, Die-Down

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Intel’s Folded Stack Chip Scale Package
For Mixing Logic and Memory
Renesas Stacked Packages for Memory

- Thin packages that can be mounted in portable electronics and memory cards. (3mm/layer)

- Packages are designed to mount one on top of another to form a “Package Stack”.

- Mix of different memory types: Flash, SRAM, DRAM, mobile RAM.

- Mix of memory and logic (processor, ASIC, controller).

- Enables testing of layers before stacking.

Source: Renesas
GE GRC 3-D Stacking Technology

Based upon the Chip-on-Flex (COF) bare chip interconnect technology

3-D Stack with 50 Circuit Layers and 8000 Array Pads
GE GRC 3-D Stacking Technology

1) Thick COF Panel
2) Thinned COF Panel
3) Sawed COF Panel
4) 1\textsuperscript{st} & 2\textsuperscript{nd} COF Circuit Stack
5) Adhesive Layer
6) 3\textsuperscript{rd} COF Circuit Being Placed

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GE GRC 3-D Stacking Technology

Array Chip Assembly to Stack

1) Apply Solder Mask
2) Pattern Solder Mask
3) Solder/Conductive Adhesive Deposition
4) Align and Place Array Chip
5) Reflow/Cure Attach
6) Repeat for Bottom Side Attach
GE GRC 3-D Stacking Technology

- 8000 polymer bumps on 200 mm pitch
- mates with 8000 element array sensor
- 17 mm by 20 mm footprint
- Silicon sensor ICs assembled onto flex and thinned to 200 µm
- 3-D stack formed by bonding 50 slices of thinned COF circuits
- flex used to connect slice edges and form area arrays
In Summary, Portable Electronic Systems Drove Packaging Technology to:

• Move packages from leaded to area array to reduce package sizes and support faster clock rates.
• Move to Chip Scale Packages to reduce size and costs.
• Develop fine line organic substrates to extend the interconnect density.
• Go to Multichip Packages to save area and to support higher frequency RF devices.
• Developed 3-D Stacking to increase circuit density.
• Develop alternates to solder balls for tighter pitch and lower cost (ICA, ACA, Stud Bumps, Floating Pads).
Advanced Packaging Technology for Leading Edge Microelectronics and Flexible Electronics
Part 3

Ray Fillion
GE Global Research
Lets Look at Embedded Chip Technologies and Thin, Flexible Electronics

- Flexible electronics are generally based on a thin film polymer interconnect structure or flex.
- Includes both active and passives components.
- These include thinned inorganic and/or organic semiconductors.
- These can be incorporated into a system or they can be the system.
- Includes mix of device types, digital, analog, RF, MEMS.
Flexible Electronics

• A key element of flexible electronics is thin film polymer interconnect structure.

• Material choices include polyimides, BCB, BT resin, LCP, epoxy resins.

• Need to have multi-level interconnects with reasonably small features (25 – 50 μm).

• Power levels are generally low.

• Need to incorporate integral, thin film passives to minimize complexity.
Flexible Interconnect Circuits
Semi-Additive, Multilayer Flex Interconnect Process Flow

1a Top side, double sided flex
1b Adhesive layer
1c Bottom side, double sided flex

2 Top & bottom flex layers laminated together with adhesive layer

3 Through hole drilled through four layer structure

4 Seed metal deposited in through hole

5 Thick metal plated up in through hole
Semi-Additive Double-Sided Flex Interconnect Process Flow

1. Pre-Preg with thin Cu Seed layer
2. Thru-Hole formed thru dielectric
3. Photo-resist applied & photo-defined
4. Thick Cu pattern plate up
5. Remove photo-resist
6. Etch exposed seed metal
NEC Multi-Layer Thin Substrate (MLTS)

Multiple Layers of Resin, Vias, Cu Traces Fabricated on Thick Cu Plate for Dimensional Control

Cu Plated Etched off to Complete Interconnect

Source: NEC
NEC Multi-Layer Thin Substrate (MLTS)

Wiring Line Layer

LSI Bonding Pad

Aramid-reinforced Epoxy Resin

BGA Land

Via-hole

Source: NEC
Baseline GE Flex Capability

• Resolution Capabilities:
  - 1 to ½ mil line and space
  - 1 mil via, 2 mil catch pad
  - 1 mil polyimide film

• Performance characteristics:
  - Metal adhesion > 8 lbs/in
  - Ti/Cu metallurgy
  - Solder mask
  - Top Ni/Au Metal
  - Thermal cycle reliability
    > 1,000 cycles (-65 to 150°C)
GE Embedded Chip on Flex with Passives

Typical mixed technology MCM applications can have a few chips and a hundred or more passives.

Integral passives can significantly reduce parts count, save cost, shrink module size and improve reliability.
Integral Resistors of Flex

Thin Film Resistors:
- $\text{Ta}_2\text{N} @ 250\text{Å} & 1000\text{Å}$
- 25 ohms/sq & 125 ohms/sq
- Range: 1K to 30K ohms
- TRC: 75 ppm/ºC
- High Frequency: >10GHz
- Dissipation: 125mW without heat sinking
- Tolerance: 5% to 1%
- Yields: > 99%

Five resistor test elements

High frequency test vehicle
Integral Capacitors on Flex

Thin Film Capacitors:
- Ta$_2$O$_5$ (Sputtered & CVD)
- 210 nF/cm$^2$
- Range: 2 to 500 pF
- Breakdown: > 40V
- Leakage: < 1µA/cm$^2$
- High Frequency: >10GHz
- Tolerance: 5% to 1%
- Yields: > 99%

High frequency test vehicle

Test caps: 0.1 to 0.002 cm$^2$
Integral Inductors on Flex

Thin Film Inductors:

- Ti:Cu @ 4 µm
- 10 to 450 nH,
- up to 16 turns
- Q factors >50
- Tolerance: 5%
- Yields: > 99.9%

Inductor with Ta$_2$N resistor

High frequency test vehicle
Georgia Tech PRC Embedded Chip
PRC Nanointerconnected Embedded Actives

Reworkable Nanointerconnections

Chips Last Embedded with Plasma Formed Chip Cavity
Auburn University Flexible Modules

- Four 50 µm Chips on Flex
- 50 µm Chips Flip Attached to Flex
- 50 µm Chips with 166 µm BGA Pitch
- Silicon Chips Flex with Carrier

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Neo-Wafer Fabrication
- Au wire bonds used to form Au bumps on chip pads.
- An array of bare chips are placed in a molding frame.
- The chips are encapsulated in molding compound forming a Neo-wafer with Au bumps protruding.
- Polyimide spin coated on the top surface and cured.
- Au traces are used to route chip-to-chip and to route to the package perimeter.
- A second polyimide/Au trace layer completes the routing.
- The Neo-wafer is then thinned to ~100 µm.
IMBERA Electronics Embedded Chips

Chips Embedded in Interconnect Structure
(Thin Board or Flex)
Fraunhofer IZM Chip-in-Polymer (CIP)

Chip-in-Polymer with Encapsulation Using Photo-definable Resin

1. Electroless Ni/Cu deposited on wafer to bond pads
2. Wafers thinned to 50 µm and diced
3. Photo-define die cavities on FR-4 PCB
4. Die placed into 40 µm deep cavities
5. Spin coat photo-definable dielectric
6. Photo-define vias to chip pads and PCB
7. Additive electroless Cu connects the chip to the PCB
8. Solder mask, electroless Ni/Au define the topside BGA solder pads
IMEC (Belgium) Embedded Chip RF

Embedded Thinned Chips

1. Integral thin film resistors, capacitors and inductors formed on BCB spin coated on a Si Substrate
2. Thinned chips mounted on the BCB dielectric layer using an adhesive
3. A second BCB layer encapsulate the chips and planarizes the surface
4. Vias are formed to the chip pads
5. Cu plated onto BCB and in vias and subtractively patterned

Interuniversity MicroElectronics Center, Leuven, Belgium
GE Thinned Embedded Chip on Flex

If Required by the Application, COF Panels Can Be Thinned to < 100 µm (50 µm Si, 50 µm Flex)
Flexible Electronics

Self Assembly on Flex
  • Inorganic elements on organic films

Electro-active "Inks"
  • Organic semiconducting inks for high-volume, low-cost processing

Mixed Organic/Inorganic
  • Combined self-assembly and organic inks
Self Assembly of Inorganic Semiconductor Elements on Flex
Printable electronics has been rapidly developing in recent years.
DOD Applications of Flexible Electronics

**Lightweight, foldable phased array antennas**
- Directed satellite communication: low power consumption with less chance of enemy interception

**Flexible Displays**
- Large, rugged screen rolled into compact, lightweight package.

**Thru-Wall Imaging**
- Locate camouflaged targets.

**Smart Camouflage**
- Rapidly adapt vehicles, personnel to surrounding environment.
Pyramid shaped Nanoblocks™ are created by chopping up a silicon wafer covered with transistors, or circuits.

A flexible plastic substrate embedded with smart electronics emerges from the process. Left-over blocks can be used to reduce waste.

Cluster of 200 LEDs

Ray Fillion, GE Global Research - Slide 26
• Patterned substrate is passed through hydrocarbon adhesive-water interface

H. Biebuyck et al., Langmuir, 1994
Capillary Forces

- Separate surfaces into hydrophobic and hydrophilic regions
- Match hydrophobic binding sites
- Coat substrate sites selectively with hydrophobic liquid
Single crystalline micro-mirrors self-assembled with hydrophobic and hydrophilic forces, onto surfaced micro-machined actuator for adaptive optics application.
Formation of Organic Semiconductors with Electro-active "Inks" on Flexible Films
Organic Transistors on Flexible Films

Carbon-based components offer the possibility of developing a wide range of very low cost electronic components and circuits all on the same substrate using high mobility organic semiconductors, suitable for use in Field Effect Transistors.

Organic polymeric semiconductors issues:
• Polymers with the correct electronic properties
• Developing stable materials
• Manufacture reproducible materials batch to batch.
• Meeting device performance requirements
  • the molecular structure of the semiconductor,
  • the material purity,
  • the surface morphology at the semiconductor and insulator/electrodes interface
  • dielectric properties of the insulating layer
PARC Polymer Thin-Film Transistors for Flexible Electronics

Ink Jetted Transistors

Palo Alto Research Center

raised feature

capillary action
MIT Organic Circuit Technology

Present Focus is on Development of Organic ...  
- LEDs  
- Lasers (Optically and Electrically Pumped)  
- Solar Cells and Photodetectors

Next Steps ...  
- Transistors and Chemical Sensors  
- Nano-Patterned Structures  
- Molecular Quantum Electronics  
- Nano-Structured Opto-Electronic Systems
MIT Organic Circuit Technology

Low-Cost All-Polymer Integrated Circuits


LAYOUT

- 3 mm

I_D - V_D RESPONSE

-15 bit programmable code generator
- 326 all-polymer transistors (2μm x 1mm gates) with vertical interconnections
- \( \mu_{\text{channel}} = 3 \times 10^{-4} \text{cm}^2/\text{Vs}, \) 40-200 Hz bandwidth
- 3" diameter polyimide substrate
MIT Organic Circuit Technology

Organic Materials ... TWO GENERAL CLASSES

POLYMERS

Attractive due to:
- Integrability with inorganic semiconductors
- Low cost (fabric dyes, biologically derived materials)
- Large area bulk processing possible
- Tailor molecules for specific electronic or optical properties
- Unusual properties not easily attainable with conventional materials

MOLECULAR MATERIALS

But problems exist:
- Stability
- Patterning
- Thickness control of polymers
- Low carrier mobility

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MIT Organic Circuit Technology

The future of organic electronics
UC Berkeley Organic Electronics Program

Close-up of high-Q inductor on plastic

Close-up of capacitor, showing 2 layers of gold separated by 100nm of polyimide. We have also developed a high-K printable material (K ~ 60)

Plastic-Compatible Low Resistance Gold Nanoparticle Conductors for Flexible Electronics
UC Berkley Organic Transistors on Fabric

- Conductive gate line
- Dielectric coating
- Active layer coating
- Weave-patterning of source and drain (A)
- Cross-woven contacts (B)
Combined Organic and Self-Assembly Inorganic Semiconductors on Flex
GE GRC Roll-to-Roll Flexible Electronics Program

High value substrates
• Pre-treated to enable electronics fabrication & barrier protection

Electro-active "Inks"
• High-value electronic inks for high-volume, low-cost processing

Enabling Technology
• Unique processes that enable manufacture of high performance devices
GE GRC Roll-to-Roll Flexible Electronics Program

OLED Lighting
Organic Photovoltaics
Flexible Sensors
Distributed/Wearable Electronics
GE Surface-Tension Self-Assembly

Key Limitations:
• Relatively low yield (~95%)
  • Sensitive to atomic level surface contamination
• Difficult to scale building blocks below ~ 100 um.
  • Small blocks stick together (hydrophobic-hydrophobic interaction).

Aggregate results:
• Demonstrated passive matrix display using LED blocks
• Alignment accuracy as good as 0.2 um.
Potential Markets: Flexible Electronics

GE Advanced Materials
- Slurries of functionalized Silicon.
- Compatible flexible substrates

GE Consumer and Industrial
- Specialty lighting
- Signage

GE Health Care
- High-performance x-ray detectors
- Ultrasound transducers

GE Security
- Large-area bio-chemical sensor arrays
- Phased-array antennas

GE Transportation
- Aircraft sensor arrays (Eddy current NDT)
- Other sensor arrays
- MEMS arrays
- Phased-array antennas

GE Consumer and Industrial
- Specialty lighting
- Signage

GE Health Care
- High-performance x-ray detectors
- Ultrasound transducers

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- Large-area bio-chemical sensor arrays
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- Aircraft sensor arrays (Eddy current NDT)
- Other sensor arrays
- MEMS arrays
- Phased-array antennas

GE Advanced Materials
- Slurries of functionalized Silicon.
- Compatible flexible substrates
Flexible Electronics

Today most commercial examples of flexible electronics involve inorganic active elements assembled or self-assembled with thin film deposited interconnects and passives on flex.

Organic semiconductors are generally limited to OLEDs and photo-voltaics except for academic and industry research laboratories.

The future will have organic, flexible electronics that can be wearable, low cost and pervasive.
Thank You for Your Attention

Ray Fillion
GE Global Research
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