Aspects of Plating for Organic Substrates

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Overview

General fabrication strategies
Circuitization:
  Subtractive processing
  Semiadditive processing
  Build-up

Aspects of selected processes
  Plating Fundamentals/Systems
  Etching
General References

Microelectronics Packaging Handbook

_Tummala and Rymaszewski_, Eds

  o Electrochemical Fundamentals/Modeling Corrosion:
  First edition Chapter 5, Second Edition I-436ff

  o Additive and Subtractive Circuitization Processes:
  First Edition Chapter 12, Second Edition III-304ff

Principles of Electronic Packaging

_Seraphim, Lasky and Li_, Eds.

  Chapter 16 General Plating -- both electroless and electrolytic
  Chapter 18 Metal Etching

Also see:

M. Paunovic, M. Schlesinger, Fundamentals of Electrochemical Deposition

G. Mallory, J. Hajdu, Eds, Electroless Plating
Plating used to make conducting connections x, y and z and to provide surface finishes for soldering or corrosion prevention.

Circuit boards (organic substrate):
   Signal traces, through vias (some v. high aspect ratio), blind vias. Employs catalysts/electroless copper and lamination most often.
   Two sided processing.

Wafers (inorganic substrate):
   Traces ~ trenches and blinds.
   Initiated with dry deposition.
   One sided processing.

Flex (organic substrate):
   Signal traces, through vias, blind vias.
   Most often uses sputtered metals for first layer and commoning.
   Commonly one sided, can be two sided processing.
Circuitization Sequences:
- Subtractive or print and etch
- Semiadditive
- Build-up

**Subtractive Processing:**
- Particularly useful for one sided circuitry.
- May be coupled with full panel plating of vias.
- Simplest process sequence, line shapes not as desirable

Copper clad substrate

![Diagram showing copper clad substrate with dielectric layers and drill through vias.]

Drill through via
If 2 sided connection
Subtractive, continued

Sputter commoning layer for through via

Full panel electrolytic copper plate. Format = mounted piece or roll

Apply/expose/develop photoresist —tent or plug holes

Etch copper, strip resist
Semiadditive Processing

Often used for processing requiring electrolytic surface finishes.

Fine line applications for chip carriers and flex.

More complex processing than subtractive.
For plating, need thin copper as an electrical commoning layer.

For flex this is most often provided with sputtered copper over a “tie” layer of Ti, Cr, Nichrome, etc. put down for adhesion.

Often the substrate dielectric is activated with a dry process to create surface active functional groups to bond to the tie layer. This can be done in a roll format.

Example: Polyimide (Kapton H)
untreated 20-24 g/mm for Cr tie layer
O2 MW plasma (reactive neutrals) 16 g/mm for Cr
O2 dc glow (neutrals+ions+photons) 50-67 g/mm for Cr
Ar ion beam (ions only) 53-58 g/mm for Cr
Concomittant water wetting angle reduction observed.

(Egitto and Matienzo, IBM J Res Devt, 1994)
Semiadditive

Organic substrate

Drill

Adhesion promote
Sputter tie metal,
Sputter commoning copper

Apply, expose,
develop photoresist

RHM
Semiadditive

Pattern electroplate copper

Strip photoresist

Flash etch commoning and tie layers

Plate protective finish Ni/Au, Sn, Sn/Pb

Strip photoresist Etch commoning and tie layers

Minimizes attack on Cu
Interconnect Schemes:

1. Core and subcomposite lamination interconnect by through hole drilling/plating. Most common for PWB. Leaves stubs at through hole interconnects.

2. Build-up processing. Often used for organic chip carrier applications. Exploits laser drilling or photovia formation. Sequential process requires high yield in later process steps.

External copper
Prepreg
Circuitized core
Prepreg
Circuitized core
Prepreg
External copper

Laminate, drill

RHM
Build-up on core or flex, two sided shown

- Laminate dielectric, etch or peel carrier if needed.

- Laser drill, 25-100 micron vias
Sputter, photo, plate, strip, flash etch

Or sputter, plate, photo, etch, strip

“1 + 1”

Wiring channel not blocked

Repeat

“2 + 2”

RHM
Parallel processing allows culling of defective cores—esp. important as the surface area of the workpiece increases.

Parallel vs. Sequential Process Yields

Graph showing the comparison between Parallel and Sequential process yields with different layer counts. The graph demonstrates that parallel processing maintains a higher overall yield compared to sequential processing, especially as the number of layers increases.

Assumes layer joining yield = 1 - (1 - layer fab yield)/4
Types of Plating

Plating is the deposition (electrochemical reduction) of metal ions from solution

1. Electrolytic plating (electroplating)
   • Uses electrical circuit to reduce (deposit) metal ions.
   • requires that the substrate be electrically conductive and that all features be "commoned", that is electrically connected.
   • Underlying chemistries and manufacturing operations are relatively straightforward.

2. Electroless plating (autocatalytic, chemical)
   • uses chemical reaction to reduce (deposit) metal ions.
   • does not require substrate to be electrically conductive.
   • does not require features to be commoned (connected).
   • does require that the dielectric substrate be catalytic for chemical reaction (use of seed or catalyst on most substrates.
   • more flexible processes
   • underlying chemistries and manufacturing operations are more complicated

3. Immersion plating (displacement)
   • Metal ion is reduced from solution by exchange with metallic substrate
   • Type of metal that can be deposited is dependent both the metal substrate and the metal ion in solution (Electromotive Series)
   • Thickness limited typically to tens of microinches (< 0.5 microns).
General Principles of Plating for Electrolytic, Electroless and Immersion Plating

Main principle of plating, regardless of type:
Some source supplies electrons for the reduction of metal ions from solution.

Metal deposition is an electrochemical reduction

$$M^{z+} + Ze^- \rightarrow M^0$$

Metal ion electrons deposited metal

Metal ions in solution are surrounded by a shell of molecules or ions called “ligands”. During the deposition process these leave the vicinity of the metal ion. The ligands may be water molecules:

$$\text{Cu(H}_2\text{O)}_6^{2+}$$
Schematic Representation of Metal Deposition

**FIGURE 16-1**
Schematic representation of the mechanism of metal deposition.
Controlling Factors

Thermodynamics:

The change in free energy, $\Delta G$ must be negative.

The free energy change can be related to the change in the electrochemical potential for the overall reaction.

$$\Delta G = -nf\Delta E_{\text{rxn}}$$

Chemical/Electrochemical Kinetics:

The kinetics of the reactions must be fast enough to yield a substantial deposition rate.

Mass transfer/Hydrodynamics:

Material must reach the plating surface (or leave the surface) by migration, diffusion, or solution flow.
The rate and overall performance of a plating system can be dependent on:

- chemical composition (ligands, pH, etc)
  - the more strongly complexed an ion, the harder it is to reduce
  - pH can affect complexation and overall chemical and electrochemical reactions

- physical properties (temperature, agitation, or mass transport)
  - high temperature and agitation results in higher rates and uniformity

- electrochemical properties of the metal ion
  - the standard potential, $E_0$
  - the charge on the ion, $Z$
  - the rate of electron transfer
Silver ion is easier to reduce than cupric ion. If a solution contains both metals, silver will be plated out first, since the std potential for silver is less negative than for cupric ion. Also, if there are no side reactions, it will take twice the number of electrons to reduce the same number of copper ions as silver ions.
Basic Principles of Electroplating

Faraday’s law: The mass of the metal plated is directly related to the number of coulombs passed through the solution. Electroplating is typically done at constant current, so that

number of coulombs = I x t

related to number of moles by Faraday constant and the number of electrons per mole of deposited metal:

Moles = coulombs/(F x n) = I x t/(F x n)
Weight of deposit = moles x atomic weight

Faraday’s law assumes 100% current efficiency, i.e., the simple stoichiometry between electrons and metal ions described by the plating reaction.
**Current Efficiency:**  the percentage of the current which goes to the useful plating reaction.

Reduction of protons to hydrogen gas is a common side reaction—car battery.

**Cell Overpotential:**  The voltage required beyond the thermodynamic potential to reach a particular current.

Plating systems are set up to have low overpotential to minimize side reactions and low current efficiencies.
Electrolytic plating uses dc current and other wave forms to deposit the metal from solution

Non precious metal baths are usually constructed with anodes that dissolve to keep the concentration of the metal at a constant value, making the baths self-replenishing.

Anode: Pb $\rightarrow$ Pb$^{2+}$ + 2e$^{-}$  Anode is electrode at which oxidation occurs

Cathode: Pb$^{2+}$ + 2e$^{-}$ $\rightarrow$ Pb  Reduction occurs at cathode (workpiece)

Copper plating systems: In organic boards and chip carriers, by far the most important system is "acid" copper.

- High throwing power, especially with reverse pulse current application
- Excellent ductility
- Can be used for either pattern or full panel plating
- Used for vertical, horizontal and in-line plating equipment

Flex circuits may also be processed in a roll to roll format.
Components of Acid Copper Baths

Copper sulfate: source of copper

Sulfuric acid, pH = -0.3 to 0.5: provides conductivity

Hydrochloric acid: enhances reduction and forms film on anodes

Additives:

1. Carriers: polyethers or polyoxyethers, which adsorb on the surface and limit access by other additives. Helps increase throwing power into holes

2. Levelers: Adsorb on edges and irregularities suppressing plating. Typically organic nitrogen compounds (amines, amide surfactants)

3. Brighteners: Sulfur containing compounds, influencing grain structure
Advances in additives and current wave forms have now allowed the filling of blind microvias

- Bubble undesirable, although not reliability issue.
- Copper filling of blind vias at lower build-up layers enables vertical stacking.
Periodic reverse pulse plating has increased the productivity and especially the throwing power of electrolytic acid copper plating baths.

See, for example G. Milad, Printed Circuit Fabrication, 20, 1997, p36
A myriad of variables available to the plater:
  - current settings
  - pulse durations
  - frequency
  - additive concentrations
  - agitation

Needs to be optimized for the application—high aspect ratio
paths not the same as blind vias not the same as fine lines.

Proper balance of wave form and additives needs to be established,
process control of the additives becoming more important.

Proper balance of wave form and additives needs to be established, process control of the additives becoming more important.

FIGURE 3. Low current density results.

Poor thermal cycling performance.

FIGURE 4. Aspect ratios of 20:1 have now been achieved using PRP.

New chemistries have come from the need to fill trenches in silicon fabrication. The microvias in chip carriers and flex packaging now reaching the dimensions where similar mechanisms are operative.

Strongly adsorbing leveller, suppressing rate at surface

Curvature-enhanced accelerator coverage (CEAC) mechanism:

Workpiece is predipped into a plating catalyst.

Geometric effects cause the catalyst to increase in concentration at acute curves as the plating proceeds. The catalyst overrides the action of a suppressor, leading to superfilling of small vias. Plating rate vs. additive concentrations critical.

**Electroless** plating systems involve the reduction of a metal ion by a chemical agent.

Basic overall reaction for an electroless plating scheme:

\[ \text{M}^{2+} + \text{Red} \rightarrow \text{M}^{0} + \text{Ox} \]
metal ion + reducing agent \rightarrow metal + oxidized form of the reducing agent

Example:

Formaldehyde used as reductant in most electroless copper baths

\[ \text{Cu}^{2+} + 2\text{H}_2\text{CO} + 4\text{OH}^{-} \rightarrow \text{Cu} + 2\text{HCOO}^{-} + 2\text{H}_2\text{O} + \text{H}_2 \]
## General Formulation of Electroless Systems

<table>
<thead>
<tr>
<th>Component</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>metal salt</td>
<td>source of metal to be plated</td>
</tr>
<tr>
<td>complexing agent</td>
<td>helps keep metal ions in solution</td>
</tr>
<tr>
<td>reducing agent</td>
<td>supplies electrons for metal ion reduction</td>
</tr>
<tr>
<td>buffer</td>
<td>helps maintain pH</td>
</tr>
<tr>
<td>stabilizers</td>
<td>retards homogeneous reactions</td>
</tr>
<tr>
<td>accelerators</td>
<td>increases rate of deposition</td>
</tr>
<tr>
<td>surfactants</td>
<td>helps remove evolved gases and increases &quot;wetting&quot;</td>
</tr>
</tbody>
</table>
Electroless Surface Finish Systems

Electroless Nickel (+IAU)
Ni(citrate)/hypophosphite: NiP deposits
Ni(citrate)/DMAB or borohydride: NiB deposits
for EMI/FR applications, diffusion barriers, rates = 0.3-0.8 mil/hr

Electroless Gold
Au(cyanide)/DMAB for wirebond, rates 0.05-/01 mil/hr

Electroless Palladium (possible "universal" finish, but not widely used
Pd(amine)/hypophosphite or formate
contacts, wirebond, solder may be possible

Electroless nickel/phos + immersion gold at times gives a phosphorus-rich brittle interface. This is called ‘black pad’.
Immersion Plating: Displacement reaction in which the substrate metal dissolves as the solution metal deposits.

Thin coatings only. “Self-limiting” is really only great slowing of rate.

\[ \text{Ni}^0 + 2\text{Au}^+ \rightarrow \text{Ni}^{2+} + 2\text{Au}^0 \]

Phosphorus does not dissolve and becomes concentrated at surface.
Etching: Removal of a material from a substrate by dissolution.

For metals, this is done by use of an oxidizing agent in solution, and is the opposite of the plating reaction.
Schematic Representation of Metal Deposition

FIGURE 16-1
Schematic representation of the mechanism of metal deposition.
Key Factors for Wet Etching

Thermodynamics: Cell reaction must be favorable

Kinetics: Rate must be sufficient to be completed within a reasonable time.

Hydrodynamics: Transport of the solution to and from the surface must be efficient to provide oxidizing agent and remove metal ions.

Anisotropy: Rate of reaction in various directions can be different depending on the hydrodynamics and additives.
Thermodynamic example: Can copper be etched with ferric chloride in hydrochloric acid solution?

Examine the cell potentials:

\[ \text{Cu}^{2+} + 2e \rightarrow \text{Cu}^0 \quad E = +0.337 \text{ V} \]

\[ \text{Fe}^{3+} + e \rightarrow \text{Fe}^{2+} \quad E = +0.770 \text{ V} \]

Net reaction: \[ \text{Cu}^0 + 2\text{Fe}^{3+} \rightarrow \text{Cu}^{2+} + 2\text{Fe}^{2+} \]

\[ \Delta E = E_{\text{red}} - E_{\text{ox}} = 0.770 - 0.337 = +0.433 \text{ V} \]

Potential change positive \(\Rightarrow\) free energy change negative \(\Rightarrow\) reaction spontaneous as written, so that etching occurs
Kinetics:

Four general steps in an etching reaction—the slowest determines the rate of reaction.

Transport of the oxidant to the surface (hydrodynamic/diffusion)

Electron transfer reaction—must have electrons move from the surface to the oxidizing agent.

Movement of the metal ion and reduced etchant from the surface

Complexation of the metal ion (avoid passivation at the surface)

\[ \text{Ti} + 4\text{H}^+ \rightarrow \text{Ti(IV)} + 2\text{H}_2 \] in sulfuric acid thermodynamically favorable, but blocked by TiO2 on the surface.

\[ \text{Ti} + 4\text{H}^+ + 6\text{F}^- \rightarrow \text{TiF}_6^{2-} + 2\text{H}_2 \] in HF solution, the titanium is rapidly etched due to complexation by fluoride ion.
Some Elements of Etching.

Etching and Photoresist or Other Etch Stops:

Anisotropic etching—high etch wall angles
  o high fluid impingement
  o banking agents

Isotropic etching—low etch wall angles
  o lower fluid impingement
  o promoted by thicker photoresist
Subtractractive resolution limited by
  o  photoresist thickness/resolution,
      conventional rule of thumb was 1:1
  o  copper thickness
  o  etch tooling

Line and space needs for chip carriers and flexible connectors
now driving down to 25 micron line and space, with
inquiries coming in at 10-15 microns for flex.
High resolution photoresists becoming available with higher than 1:1 aspect ratio of the line channels. Resist below is 25 micron thick. Drives some of the geometry issues into etching and plating.

L/S=8/8 micron Resist pattern profile with New High Resolution DFR

M. Oda, R. Barr, A. Hinata, C. Keil, T. Yamamoto
www.nichingo-morton.co.jp
Common Copper Etchants

Cupric Chloride/Hydrochloric Acid:

\[ \text{CuCl}_2 + \text{Cu} \rightarrow 2 \text{CuCl}_\text{s} \overset{\text{Cl}^-}{\rightarrow} \text{CuCl}_4^{3-} \]

The cupric ion is regenerated with air and reused. System compatible with most photoresists

Ammoniacal Alkaline

\[ \text{Cu(NH}_3)_4^{2+} + \text{Cu} \rightarrow 2 \text{Cu(NH}_3)_4^+ \]

Key use for flash etch for tinned or nickel/gold plated features

Persulfate Ion:

\[ \text{S}_2\text{O}_8^{2-} + \text{Cu} \rightarrow \text{Cu}^{2+} + 2\text{SO}_4^{2-} \]

Key use is for microetching