The technique of reducing the number of levels of a package, as is done in low-cost systems, may also be used in building the largest systems. In this case the chip carrier containing a single chip is replaced by a complex, large multichip module (Figure I-4, Introduction) in which the chips are packaged very close together [7]. Since 100 or more chips are packaged on each module, the need for cards and conventional printed circuit boards is eliminated. The large modules are plugged directly into a back panel planar [9,10]. The planar provides the printed circuit cabling between the modules. Since many chips are placed very close together in this type of planar package, electronic signal transit time is greatly reduced [11]. However, the interface requirements, particularly heat removal, become very difficult to meet because of the increased circuit density. Furthermore there is a demand for a large number of connections between the module and the back panel, driven by the need for communication between the large number of circuits contained on each module. In the case of the IBM 3081 processor, each module contains about 30,000 circuits and requires 1800 connector contacts for power and signals. Thus the connector contact system becomes complex. To achieve the large number of interconnections between each module, the printed circuit back panel (Figure 2-1) becomes very complex. The factors that influence these interfacial considerations will become clear as we discuss each component in this chapter [2,12,13].

ELECTRICAL INTERCONNECTIONS BETWEEN PACKAGING LEVELS

The primary function of the interface is to provide the electrical interconnection between the two levels of packaging. The number of terminals required is related to the communication needed between a given component and the rest of the system. Thus, as the function within a component increases, so do the number of inputs, outputs, and controls, including, in some cases, test points required to guarantee the function. Packaging engineers work toward promoting growth at these interfaces.

As noted earlier, interfacial growth is driven by the functional increase at the semiconductor chip. The number of terminals increases as a power function of the number of circuits. This relationship was discovered in 1960 by IBM engineer E. Rent when he plotted the number of input-output lines against the number of circuits in the cards of the IBM 1401 computer [14]. This relationship can be expressed as

\[ I = bC^p \]

where \( I \) is the number of I/O lines, \( b \) is a constant, \( C \) is the number of circuits on a package, and \( p \) is a positive exponent.

In Rent’s original work, \( p \) was found to be approximately equal to \( \frac{2}{3} \) while \( b \) was about 2. Figure 2-2 shows a relationship similar to Rent’s. However, this figure is a plot of the number of I/O connections versus the number of
circuits across many technologies, whereas Rent's work applied to the hierarchy within a given system. That is, his relationship is concerned with the number of I/O connections at each packaging level within a given system. When a plot is made for various components across different technologies as we have done, the exponent is much lower than the $\frac{2}{3}$ found by Rent but the constant $b$ is much higher.

The Rent relation can be derived heuristically based on the arrangement of circuits on a chip. For example, a circuit has several inputs and outputs. Accordingly, the intercept at one circuit should represent the number of signal leads for an average circuit, which is typically in the range of three to five. Let us consider the case of an average of four leads per circuit. Now, consider an
The Rent trend line relating terminals to circuit function. The trend line appears to be consistent for chips, multichip modules, cards, and boards over six orders of magnitude in circuit function. The least-squares fit is $I = 6.54C^{0.435}$. The steeper line is the Rent line for various levels of packaging within a system.

array of circuits on a chip and cut out a representative square. Along one side of the square let there be $N$ circuits. Then the number of circuits within the square is $C = N^2$ and the number of circuits along the periphery is $4N$. Therefore, the number of I/Os along the periphery is related to the number of circuits within the square as

$$I = bC^{1/2}$$

where $b$ is a constant that depends on the number of I/Os per circuit. This square root rule is very interesting, since it reflects more truly the relationship between circuits and I/Os in today’s VLSI world than the $2/3$ power of Rent in the days of unit logic.

The number of terminals or wire bonds connecting a chip to the module has been increasing rapidly, and the number of pins on single-chip modules has been increasing equally rapidly. Furthermore, with the introduction of more than one chip on a module, the number of terminals on the module increases as the product of chips and terminals per chip taken to the power $p$. Characteristic of
integration increases, the terminal count hierarchy on the various levels of package is expanding at every level.

We give here relationships between the number of terminals at various levels of packaging and the number of circuits in a package based on Rent's rule.

\[
\begin{align*}
\text{Chip terminals} & = bN_c^p \\
\text{Multichip module terminals} & = b(nN_c)^p \\
\text{Card terminals} & = b(nN_c)^p \\
\text{Board terminals} & = b(mnN_c)^p
\end{align*}
\]

where \( m \) = number of cards
\( n \) = number of chips on card or module
\( N_c \) = number of circuits on a chip

With these relationships between various levels of packaging, it is possible to determine the interconnections required between them based on their circuit content. In addition to these signal I/O connections, voltage or ground connections will be required. The ratio of voltage connections to signal I/Os varies quite a bit depending on the type of package. There is commonly one voltage connection per three or four signal I/O connections. In the highest performance systems, there may be one voltage connection for each signal in order to reduce noise. That is, the adjoining voltage connections (sometimes called reference connections) act as shields to the signal I/Os.

CHIP CARRIERS OR MODULES

Along with the electrical interconnection discussed in the section above, the joining element between chip carrier and chip must provide the proper mechanical environment. The first semiconductor carriers were ceramic-based, hermetically sealed packages, called TO-5s. The back of the chip was eutectic (AuSi) bonded to the gold-coated ceramic. Thermal compression bonding of thin wires from the chip terminals (evaporated aluminum pads) to glass-sealed Kovar pins held in place by the ceramic glass seal provided a strain-relieved mechanical link. A metal can, also glass sealed, encapsulated the device from environmentally degrading reactions.

A variety of single chip carriers have gradually replaced the hermetically sealed TO-5 can [15]. Predominant among these and a standard for the industry has been the dual in-line package (DIP), constructed primarily from a metal lead frame and plastic. The chip sits on a metal ground strap for good thermal conduction while the interconnections are wire bonded from the aluminum pads on the chip to the frame leads. The entire package is then molded with plastic followed by forming of the leads. Until recently, the leads have been limited to two sides of the chip carrier, but the increased integration at the chip level (Figure 2-3) has required more interconnection. This increased interconnection