Package Interconnects

**Permanent Connections**
- Die level interconnect
- Die to package interconnect
  - Thermocompression (TAB)
  - Wirebond
  - Flipchip
- Substrate interconnect
- Card/board interconnections

**Separable Connections**
- Connectors, sockets, LGA, compliant pins, etc.
Conventional Flex Packaging

A conventional flex packaging application:

Flex provides electrical connection path between discrete functional units.

Flex cables provide either:
• product assembly convenience, or
• flexible connection in operation

JVC Camcorder (circa 1999)
Common Package Interconnections

- Die
- Wire Bond
- Flip chip solder
- Braze Joint
- Lead Bond
- OLB
- Solder
- PTH
- Contact Element
- MCC
- Interposer
- Circuit Board
- Eutectic Solder 90/10 Pb/Sn
- CTE ~ 3ppm/°C
- CTE ~ 6ppm/°C
- CTE ~ 16-21ppm/°C
Conductor Bonding Technologies

- Soldering
- Brazing
- Thermocompression Bonding
- Ultrasonic Bonding
- Transient Liquid Phase Bonding
- Adhesive Bonding
Die to Chip Carrier Interconnection Systems

Die

MCC

Wire Bond

Wire Bond

CTE ~ 3ppm/°C

CTE ~ 6ppm/°C

Interposer

CTE ~ 16-21ppm/°C

Circuit Board

Die

Flip chip solder

Braze Joint

Solder

CTE ~ 3ppm/°C

CTE ~ 6ppm/°C

CTE ~ 16-21ppm/°C

Lead Bond

OLB

ILB

Pb/Sn

Contact Element

Eutectic Solder 90/10

PTH
Die to Package Interconnect

• TAB (Tape Automated Bonding)
  – Au thermocompression

• Wirebond
  – Ball bond
  – Wedge bond
  – Interfacial (intermetallic) considerations
TBGA (Tape Ball Grid Array)

Thermo-compression Bond (Flip Chip)

- Heatsink or Coverplate
- Adhesive
- Thermal Compound
- Copper Stiffener
- 10/90 Solder Ball
- Pb/ Sn Eutectic
- Die
- Encapsulant
- Tape: Cu / Polymide / Cu
Wire Bonding – Perimeter Package

QFN

Land-Site

QFP

Gull-Wing Lead

E. McDivitt /K&S
PBGA (Plastic Ball Grid Array)

- Mold Compound
- Die Pad
- Plated Copper Conductor
- Signal / Ground Via
- Wire Bond
- Solder Mask
- BT Epoxy PCB
- Thermal / Ground Via
- Solder Bump
PBGA (‘Enhanced’) Heat-sinked Multi-layer PCB Construction Two-tier Wire Bonding

Heat Sink
Plated Copper Conductor
Prepreg
Solder Bump
Wirebonding

- BGA Solder Balls
- Substrate
- Glob Top Dam (Clear Glob Top shown)
- In-Line Die Pads
- Gold Wires
- Silicon Die
- STAGGERED SUBSTRATE BOND FINGERS
Wirebonding

- Metallurgical bond formed
  - Substrate Heat
    - promote interdiffusion of metals
    - substrate temperature 150 to 170°C
  - Pressure
    - ensure sufficient area of contact
    - 30 to 50 gms / bond
  - Ultrasonic ‘scrubbing’ of surfaces
    - break through surface oxides and contaminates
Ball Bonding

**Main Characteristics**
- Multi-directional bonding
- Bond sizes range from 2.5 to 4 times wire diameter
- Deep access with standard tool
- Used mostly with **gold** wires
- Higher bonding speed
1. Wire in capillary, ball preformed.
2. Locate position, pull ball tight.
3. Bond force, ultrasonic applied
4. Raise capillary, begin loop
5. Move away from target lead
6. Raise to loop height
7. Move relative to device
8. Squash wire with ultrasonic to form second bond
9. Raise to tail height and clamp wire
10. Raise to tear wire at chamfer
11. Stop at Reset height
12. Discharge EFO wand to form ball for next bond
Capillary Design

Capillary design is key to successful ball bonding

- Inner chamfer angle optimized for application
- Polished inner chamfer
- Matte finish face and outer radius
Critical capillary dimensions

M.Klossner, et al. /K&S
Ball bond example – no neck damage

E. McDivitt /K&S
Measured diameter of bonded ball C is closer to the actual contact diameter, producing a higher shear per unit area.

M. Klossner, et al. /K&S
Increased tail bond pull strength from post bond heating
Au Ball bond on Al pad

Intermetallic growth as a function of time at 175°C.

S. Kumar, et al. /K&S
Etched cross-section showing grain structure of Au ball and of two different grain formations of intermetallic layers (nominal strength, aged 500 hrs)  S. Kumar, et al. /K&S
Etched cross-section showing voids at the interface between Intermetallic 1 and intermetallic 2 (nominal strength, aged 500 hrs)  

S. Kumar, et al. /K&S
Wedge Bonding

Main Characteristics
• Uni-directional bonding (device or tool must be rotated often)
• Creates small bonds (1.1 to 2 times wire diameter)
• Deep access with "Deep Access" M/C and tool
• Usually used with aluminum wire
• Can easily bond without heating
Wedge Bonding

Typical tail break mode

Crescent Bond Weld length  Tail Bond Weld length

Wire Diameter

Wire clamp breaks tail

Tail bond break mode

S.Kumar, et al.
Die to Package Interconnect

• Flip Chip
  – Device Interconnect Structure
  – Solder Bumps
    • High melt (Pb-rich) C4
    • Duplex FCA solder joint
    • Low melt (eutectic Sn-Pb) C4
  – Underfill Encapsulant
    • Principles
    • Materials considerations
C4 Solder Connection

Die

Pb/Sn

C4 “Bump”

Al Capture Pad

Via

BLM

Au/Ni

Ceramic Substrate

Substrate Via
C4 - Controlled Collapse Chip Connection

- Robust assembly process
  - Collapse of solder accommodates board & bump tolerances
  - Self-alignment allows for reliable fine pitch placement
- Requires a fully reflowable solder bump

after P.Elenius /FCT
C4 Type Solder Reflow

- All required solder for the joint is on the chip
  - Typically high Pb solder for ceramic (‘high melt’)
  - Eutectic Sn/Pb solder for laminate (‘low melt’)
- High joining process yields
Flip Chip Device Interconnect

- **Final Device Metal Layer**
- **Passivation Layers**
  - Chip passivation – protects final device metal
  - C4 passivation
  - SiO$_2$, Si$_3$N$_4$, polymide, BCB
- **Terminal Metals**
  - Interconnects final device metal to chip bump
  - “Under Bump Metal” (UBM) or “Ball Limiting Metal” (BLM)
- **Interconnect Bump**
  - Solder bump (Pb3Sn, Sn36Pb, SnAg, SnCu)
  - Gold stud bump
C4 Device-side Terminal

Cross Section View:
- C4 Passivation
- Chip Passivation
- Terminal Via
- Final Device Metal Pad

Top View:
Solder Bump Flip Chip Terminal

Inter-layer metal
Inter-layer dielectric

C4 Passivation
UBM - Under Bump Metal

Solder Bump
Peripheral Pad
Terminal Via

Side View
Solder Bump UBM Requirements

• Excellent adhesion to passivation
• Excellent adhesion to final metal
  – w/ low stress levels to prevent cratering, etc.
• Low electrical contact resistance to final metal
• Solder wettable metal
• Reliable solder diffusion barrier
• Protection of final device metal from environment
• Compatibility with probed wafers

after P.Elenius /FCT
C4 Bump Structure

- C4 Polyimide passivation (4-5 microns)
- Under Bump Metal (UBM) or Ball Limiting Metal (BLM) (Au/Cu/Cr)
- Final Via
- Pb/Sn Bump
- Final metal pad 10K Å Al/Cu
- Die passivation Oxide / Nitride passivation
Under Bump Metallurgy

• Adhesion Layer
  – strong bond with passivation and terminal metal
  – Cr, Ti, or TiW
  – very thin to minimize stress on passivations

• Solder Wetting Layer
  – provides wettable surface for solder bump
  – withstand multiple reflows (diffusion barrier)
  – bond bump to adhesion layer
  – Cu or Ni

• Protective Layer (oxide prevention)
  – Au (thin, ~10’s of nm)
UBMs used for Solder Bumping

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Under Bump Metal Systems</th>
</tr>
</thead>
<tbody>
<tr>
<td>Representative of</td>
<td>FCT</td>
</tr>
<tr>
<td>Adhesion</td>
<td>Al</td>
</tr>
<tr>
<td>Diffusion</td>
<td>Ni</td>
</tr>
<tr>
<td>Wettability</td>
<td>Cu</td>
</tr>
<tr>
<td>Oxide Prevention</td>
<td>n.a.</td>
</tr>
<tr>
<td>Suitable for 63Sn/Pb</td>
<td>yes</td>
</tr>
<tr>
<td>Probed Wafers</td>
<td>yes</td>
</tr>
</tbody>
</table>

after P.Elenius /FCT
Flip Chip Wafer Bumping

• **Bump compositions**
  – High melt (ceramic substrate applications)
    • Pb-3Sn, Pb-5Sn, Pb-10Sn
  – Low melt (organic substrate applications)
    • Sn-37Pb, Pb-free compositions (SnAg, SnCu)
  – “Duplex” bumps (low melt on high melt base)

• **Three primary bumping methods**
  – Evaporated UBM / Evaporated solder bump
  – Sputtered UBM / Electroplated solder bump
  – Sputtered UBM / solder paste screened solder bump
  – others include:
    • decal transfer, solder ball placement, solder jetting,
Evaporated UBM and Solder Bump

Process Flow
- Spin on passivation
- Pattern and open passivation
- Evaporate UBM thru metal mask
- Evaporate Pb/Sn solder thru metal mask
- Reflow to ball solder bump

Polyimide Passivation 4-5 microns

Die Passivation

UBM – (Cr/Cr-Cu/Cu/Au) or TiW/Cu/Au

Sn

Pb

Pb/Sn Solder Bump (97/3 or 95/5) typically

after P. Elenius /FCT
As-Deposited Evaporated UBM Stack

- Solder Terminal
- Device conductor
- Al-based alloy
- Lead-rich solder
- Sputtered SiO$_2$
- Silicon
- BLM
- Tin rich cap
- Phased Cr-Cu
- Free Cu
- Au
- after P.Elenius/FCT
Cr/(Cr-Cu)/Cu/Au  UBM

- Good adhesion to final metal and passivation
- High stress thin film
- Solderable layer provided by the Cu/Au
- Cr-Cu is solder wettable diffusion barrier
  - Cu is quickly consumed by 63Sn/Pb solders
  - Very poor UBM reliability with 63Sn/Pb and other high Sn bump compositions
- Capable of 20+ reflow cycles with 97Pb/Sn

after P.Elenius /FCT
Evap Bump: Before/After Reflow
Evaporated UBM after Reflow

Silicon

Sputtered SiO$_2$

BLM

Homogenized Pb/Sn Solder

AuSn Intermetallics

Sputtered SiO$_2$ Passivation Layer

Phased Cr/Cu

Cr

Free Cu (if any)

Intermetallic Cu$_x$Sn$_y$
Cr/(Cr-Cu)/Cu/Au UBM Stability

Interface with eutectic Sn-Pb at 200°C
Evaporated UBM and Solder Bump

- Expensive Process
  - Metal shadow mask or in-situ mask
  - Precision mask alignment for metal masks
  - Large, expensive and slow evaporators
- High Pb Solder Alloys Only
  - Sn vapor pressure very low
- Significant quantity of Pb waste
  - Low alpha solder cost increase
- Pitch limited to 200 microns

after P.Elenius /FCT
Sputtered UBM and Electroplated Solder Bump

One option shown; 4 to 5 common in practice

Pb/Sn Pad (95/5, 90/10 or 37/63)

Die Passivation

Thick Cu plated-up layer (stud)

Sputtered UBM - (TiW/Cu/Au)

Final Metal Pad

after P.Elenius /FCT
Sputtered UBM and Electroplated Solder Bump

Process Flow
- Sputter UBM over entire wafer
- Apply photo-resist, pattern, develop
- Electroplate thick copper layer (stud)
- Electroplate solder
- Strip photo-resist
- Etch back UBM to solder bump
- Reflow to form solder bump

after P.Elenius /FCT
TiW/Cu/Au   UBM

• Variable adhesion to final metal and passivation

• Cu provides solderable surface
  – Copper is consumed during reflows
    • more rapidly consumed with high tin content solders

• TiW is not a solder wettable diffusion barrier
  – Limits the number of reflow cycles

• Higher stress thin film

after P.Elenius /FCT
Sputtered UBM and Electroplated Solder Bump

• Lower cost than evaporated process
• Pitch capability is <100 microns
• Electroplated solder metallurgy
  – Limited compositional control
  – Excessive height variation across the wafer
  – Cu stud reduces reliability
  – Significant voiding is typical
• Limited to binary solder alloys

after P. Elenius /FCT
Sputtered UBM and Solder Paste Bump Processes

**Process Flow**
- Sputter UBM over entire wafer
- Apply photo-resist, pattern
- Etch UBM to form cap
- Deposit solder paste
- Reflow to form solder bump

Sputtered UBM - (Al/NiV/Cu)

Solder Bump (variety of alloys)

Final Metal Pad

Die Passivation

after P.Elenius /FCT
Al/Ni(V)/Cu / eutectic Sn-Pb

No intermetallic spalling

(a) as received, (b) 1 min, (c) 5 min, (d) 10 min, (e) 40 min at 220°C

K-N Tu / UCLA
Al/Ni(V)/Cu UBM

- Excellent adhesion and electrical contact with Al
- Ni(V) is excellent solder diffusion barrier
- Initial solderable layer provided by the Cu
- Lower stress thin film
- Can bump over probe marks
- Qualified for up to 10 reflows @ 240°C
  - With 63Sn/Pb solder
Sputtered UBM and Solder Paste Bump Processes

- Lower cost than evaporated process
- Solder paste processes allow
  - Excellent metallurgical control
  - Bumping with non-binary solder alloys
    - lead free solders
- fine pitch possible (<150 micron)
  - Pressure screening head

after P.Elenius /FCT
Bumping - Electroless Nickel

- Electroless Ni UBM/Bump with Au Flash
- Die Passivation
- Final Metal Pad

after P.Elenius /FCT
**Bumping - Electroless Nickel**

**Process Flow**
- Double zincate
- Electroless Nickel plate
- Immersion gold

**Next Step**
- Use as is with conductive adhesives
- Transfer solder to bump
  - Solder ball bumping
  - Decal bumping process
  - Solder paste

_after P.Elenius /FCT_
Electroless Ni(P) UBM

SEMATECH

K-N Tu/UCLA
Electroless Ni UBM

- Potential to be lowest cost process
- No adherence of Ni to passivation
- Al bond pad thickness is reduced 30-40%
- Very high stress film

after P.Elenius /FCT
Electroless Ni UBM

• Not solution for all wafers and/or products
  – High volume consumer & consumable possibly

• Process challenges
  – Uneven or no plating
  – Galvanic coupling
  – High film stresses
  – Long term process repeatability

• Fine pitch limitations

after P. Elenius /FCT
High melt C4 attach process cannot be used with laminate substrates.  
- 360°C reflow process destroys the epoxy laminate

High melt chip bumps can be used on laminates if soldered with eutectic SnPb.  
- 225 – 245°C reflow temperature compatible with laminate material  
- eutectic Sn-Pb solder must be supplied to joint, usually on the carrier pad  
- some technologies for supplying eutectic directly on tip of bump
FCA Chip Joint Structures

Pb-3Sn ‘high melt” chip solder bumps on eutectic Sn-Pb substrate deposit

Rectangular Cu trace, plated eutectic solder. Laminate SRAM package; no substrate micro-via layers

Substrate surface vias, Ni/Au plated solder paste filled
FCA Chip Joint Structures

Pb-3Sn ‘high melt” chip solder bumps on eutectic Sn-Pb substrate deposit

Circular, flat Cu substrate pad, OSP finish with liquid dispensed eutectic solder (Non-solder mask defined pad)

Plated Cu filled surface via with liquid dispensed eutectic solder deposit
FCA Solder Joints

Chip interconnections

Photo Vias

Copper Filled Vias
Low melt FCA w/ High melt Bumps

- Requires eutectic solder on carrier – cost
  - Solder electroplated, screened, or liquid dispensed
  - Mechanically flattened for coplanarity
- More prone to non-wets
  - Chip join fluxes less effective on Pb oxides
- Limited bump collapse
  - reduced accommodation of substrate non-planarity
- Less tolerant of bump damage prior to join
  - bump does not reshape itself during chip join
- Less solder joint volume expansion on subsequent refloows
  - Reduced underfill delamination stresses
- Permits multiple package options for same die
  - ceramic and organic substrates
  - single bumping line for both (same UBM and solder bump)
Bump damage prior to chip join:

- Pb-rich bumps very soft
- no problem for full melting C4
- potential interconnect open for non-melting bump attach
BSE image of C4 non-wet on laminate via.

- Not an inspectable defect
- often tests good at time-zero
- field reliability risk
Encapsulation (Underfill)

- Fills gap between die and substrate
  - mechanically couples silicon to substrate
  - maintains solder joints in hydrostatic compression
  - provides environmental protection of solder surface
- Minimizes thermally induced cyclic strains
  - substantial fatigue life enhancement (>10X)
  - enables flip chip on laminate (otherwise not feasible!)
- Materials
  - Filled (e.g., silica, alumina) epoxy
  - CTE matched to solder joint material
  - Glass transition (Tg) > 125°C
Capillary Flow of Underfill Encapsulants

Key features

- $s < 100 \, \mu m$
- particle size $< s/3$
- $\rho_s/\rho_o \sim 2$
- capillary driven

E.Cotts
Underfill Material Properties

**Uncured**

- **Dispensibility**
  - viscosity, thixotropy
- **Void free filling**
  - no volatiles (100% solids)
  - low surface tension
    - good wetting, all surfaces
  - tight filler particle size dist.
    - max particle size < gap/3
  - minimal flow segregation
- **Minimal Fill Time**
  - surface wetting
  - low RT viscosity (5-30 Pa-s)
    - decrease with temperature
  - filler particle size, shape
- **Excellent Fillet Formation**
  - silicon wetting
  - low viscosity
- **Manufacturing ‘handling’**
  - single component system
    - premixed resins, fillers, hardeners, catalysts, etc.
  - shelf life
    - 6 month min (-40°C ok)
  - pot life
    - 8 hours at ambient
Underfill Material Properties

Cured

- Modulus >3.5 GPa
- Fracture toughness >1.8 MPa√m
- Adhesion > 6.5 Mpa
  - chip passivation
  - substrate surface
- CTE (filled composite)
  - 20-40 ppm/°C (below Tg)
- Glass Transition >125°C
  - Tg above max service temp
- Low moisture absorption
- Insulation resistance >1x10¹³ Ωcm
- Dielectric constant < 4
- Low extractable ion content
  - residual Cl⁻ <5ppm
- Low alpha particle emission
- High thermal conductivity
FC / PBGA Assembled to Card
(Flip Chip / Plastic Ball Grid Array)
Underfill Fillet Reduces Stress on Perimeter C4 Joints

Fillet with Edge Crack

H.Nied, 1998
Die Underfill Failure Mode

- Initiates at encapsulant surface
  - Region of maximum tensile stress

- Solder joint failure of an encapsulated die
  - Joint deformation less
  - Occasional bulk joint failure
Underfill Failure

Die

Underfill

Fatigue Fracture

Chip Carrier
Substrate Interconnections

- Die
- Braze Joint
- Eutectic Solder 90/10 Pb/Sn
- Contact Element
- Flip chip solder
- Wire Bond
- CTE ~ 3ppm/°C
- CTE ~ 6ppm/°C
- CTE ~ 16-21ppm/°C

- Chip Carrier Substrate
- OLB
- ILB
- Circuit Board
- Solder
- PTH
Substrate Interconnects

- **MultiLayer Ceramic (MLC)**
  - Stacked via structure
  - Sintered metal conductors

- **Laminate substrates**
  - Plated copper interconnects
    - PTH
    - micro-via

- **Stacked organic substrates**
  - Interconnect schemes:
    - Electrically Conductive Adhesives
    - Transient Liquid Phase bonding
    - Solder
MultiLayer Ceramic Stacked Via Structure

9211 Alumina

sintered Mo paste vias and lines
Cordierite Glass-Ceramic/Cu Substrate

~ 70 layers
Laminate Micro-via Substrate

Encapsulation

Micro-via or ‘build-up’ layers

Die

PTH
Vertical (Z) Interconnect Substrate Via Structures

Schematic Cross Section
Approximately to scale
Vertical (Z) Interconnect Structures

Layer Interconnection with Plated Thru Holes

Lines must go around PTH's

Layer Interconnection with Vertically Terminated Vias

VTV's don't block lines
Effect of Substrate Via Structure on Chip I/O Wiring Escape

Escape through PTH Grid

Grid Escape using Vertically Terminated Vias
Z-Interconnect Substrate Fabrication

Sequential Build-Up Process

1. Fabricate Core
2. Fabricate 1st Build-up Layers on Core
3. Fabricate 2nd Build-up Layers on Existing Layers

Parallel Assembly Process

1. Fabricate All Layers Separately
2. Join & Interconnect Layers
Stacked Vias with Electrically Conductive Adhesives (ECA)

- Stacked vias with Cu filled paste in through-vias
- Ag filled electrically conductive adhesive to form Z interconnects
- Epoxy-glass Laminate
- Cu overplate for bonding pad
Electrically Conductive Adhesives

- **Isotropic Adhesives**
  - Conduct Uniformly in X, Y and Z Directions
  - Percolation Theory
    - Critical Volume Fraction
    - Short Range Coherence Length

- **Anisotropic Adhesives**
  - Conduct Only in Z Direction
ECA Percolation Path

Factors Affecting Critical Volume Fraction

• Mixing Time
  • uniformity of dispersion

• Thixotropy
  • stability of dispersion

• Filler Particle Considerations
  • particle size and distribution
  • particle geometry
    • spheres
    • flakes
    • fibers
  • agglomerates
  • total surface area

Low conductive filler content

Critical volume fraction for percolation

High conductive filler content
COMPARISON OF CONTACT RESISTANCE

CONTACT RESISTANCE IN MILLIOHMS

PERCENTILE

- - - SOLDER
- - - THERMOSET A
- - - THERMOSET B
- - - THERMOSET C
- - - YORKTOWN PMC
Anisotropic Film Bonding

- Electrically Insulating Particle
- Electrically Conductive Particle
- Flex Circuit
- Conductor Pads
- Rigid Substrate
- Bond with Temperature, Pressure and Time

ACF
Anisotropically Electrically Conductive Adhesives

- Require one adherend flexible
  - typically polyimide flex (< 0.003”)
  - uniform pressure
  - final bondline 5-10 microns
- Minimum bond area > 120 mils²
  - >20 particles in bond area
- Select ECA for circuit line width and pitch
  - Sufficient adhesive to fill space
  - Circuit line height <14 microns
- Particles CTE matched to adhesive
  - 70-95 ppm/°C
Card/Board Level Interconnect

• Pin-in-Hole
• Surface Mount – perimeter
  – Leaded components
  – Leadless components
• Surface Mount – area array
  – BGA
    • full melting solder ball (laminate)
    • non-melting ball (ceramic)
  – CCGA
    • non-melting columns
Commercially Available BGA Packages
Plastic Ball Grid Array Interconnect

Eutectic Sn-Pb BGA interconnects on laminate build-up carrier

full melting, collapsing, solder connection
CBGA / CCGA Interconnections

Non-melting balls and columns with low melting card attach

Ceramic Ball Grid Array (CBGA)

Card / Board
Solder Ball Connection

Die

MLC Substrate SCM/MCM

63Sn-37Pb

90Pb-10Sn

Ceramic Column Grid Array (CCGA)

Card / Board
Wire Solder Column Connection

Die

MLC Substrate SCM/MCM

63Sn-37Pb

90Pb-10Sn

Card / Board
Cast Solder Column Connection
CBGA Card Interconnect

90/10 Pb/Sn

Eutectic Pb/Sn

non-collapsing solder connection
Ceramic Ball Grid Array

32mm CBGA (625 I/O)

Card mounted 32mm CBGA
Dual-Solder BGA Interconnects

- Improved fatigue life over full melting joints
  - increased stand-off reduces thermally induced strain
  - high Pb alloy softer than eutectic Sn-Pb

- Allows non-collapsible column interconnect
  - further reduction of thermal strains
  - more difficult card assembly
    - prone handling damage
    - rework difficult
Ceramic Column Grid Array

44mm CCGA (1089 I/O)

Card mounted 32mm CCGA

MLC Substrate
87 mil Solder Columns
Board

90Pb-10Sn

44mm CCGA (1089 I/O)
Common Package Interconnections

- **Die**
- **MCC**
- **Braze Joint**
- **Eutectic Solder**
- **Printed Circuit Board**
- **CTE ~ 3ppm/°C**
- **90/10 Pb/Sn**
- **Contact Element**
- **Flip chip solder**
- **Wire Bond**
- **CTE ~ 6ppm/°C**
- **CTE ~ 16-21ppm/°C**
- **ILB**
- **OLB**
- **Lead Bond**
- **Solder**
- **PTH**
- **Interposer**
Environmental Product Constraints

• Global trend to restrict hazardous content in electronic products.
  – previous regulatory emphasis on manufacturing waste stream or product recycling
• European Union “Restriction of certain Hazardous Substances” (RoHS) directive effective July 1, 2006
  – restricts Pb, Hg, Cd, Cr\textsuperscript{+6}, PBB, PBDE
  – directed largely to consumer products
  – exemptions for critical applications
• Other geographies following suit (China, CA, ME, …)
Pb Elimination

- EU “Restriction of Hazardous Substances” (RoHS) directive eliminates Pb in electronics by July 1, 2006
  - exemptions for servers, medical, avionics, etc..
- Significant impact to Package Interconnects
  - elimination of Sn-Pb eutectic solder!
  - applies to most flexible electronics now in development
- Requires:
  - New solderable surface finishes
    - Sn whisker mitigation
  - New Pb-free solder alloys
    - SnAgCu ternary (near eutectic) is most common
Solidification Trajectory of SnAgCu Alloys

Diagram shows Calculated Equilibrium Liquidus Temperatures for Different Alloy Compositions.

- Sn-3.9Ag-0.6Cu, NEMI alloy
- ~Sn-3.7Ag-0.8Cu, Nominal Eutectic

[ NIST eutectic: Sn3.5A0.9Cu ]


Portion of Calculated Liquidus Projection Ternary Phase Diagram (Contour Map of Liquidus Surfaces) after E. Cotts
Nucleation and Growth of Ag₃Sn Plates at Slow Cooling Rates

Solidifying Alloys Cool Below the Meta-Stable Ag₃Sn Liquidus Line

Slower Cooling provides more time for Nucleation and Growth of Ag₃Sn Plates


Below the Meta-Stable Ag₃Sn Liquidus Line a driving force of Nucleation of Ag₃Sn plates in the liquid exists.

Sn-3.8Ag-0.7Cu Solidification:
Cooling Rate from 240°C

0.2°C/sec

Ag₃Sn plate formation at slow cooling rates.

Large supercooling (~30°C) required for Sn nucleation inhibits eutectic solidification allowing time for Ag₃Sn nucleation and growth

Ag₃Sn plate formation deplete Ag from matrix producing softer solder joint.
SnAgCu BGA: microstructures

Optical BF; SAC-ATC

SEM; SAC-ATC

Optical X-pol; SAC-ATC

SEM; SAC, >1°C/sec.

SEM; SAC, 0.3°C/sec.

E. Cotts
SnAgCu BGA mixed soldering

Reflow below SAC melt
(non-homogenous)

Sn/3.5Ag/1.0Cu Bump Assembled with Sn/37Pb Paste
Peak Reflow Temperature of 205 - 211degC
White Regions are Pb
Grey Regions are Sn
(Black "Specks" are Contaminants)

Poor Reliability

Reflow above SAC melt
(homogenous)

Sn/3.5Ag/1.0Cu Bump Assembled with Sn/37Pb Paste
Peak Reflow Temperature of 221 - 228 degC
Pb Phases (White Regions) Extend from Pad to Pad
(Black "Specks" are Contaminants)

Acceptable Reliability

Universal Instruments Consortium
Industry Pb Elimination Status

• Much of consumer electronics has converted to Pb-free solder assembly
  – cell phones, PDAs, video games, etc.
  – field reliability data still being collected
  – alloy options will narrow as technology matures
• Most flip solder joints will continue to use Pb (likely through 2010)
  – substantial materials / reliability challenges
• Server and avionics mostly opting to invoke Pb-solder exemption
  – component supply chain realities often conflict with this preference
• Emerging Flexible Electronics applications must be defined in full compliance to all global substance restrictions.