Process and performance of a-Si and poly-Si TFTs on plastic

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1. Introduction:

A major advancement in the field of flexible electronics has been the development of a method to deposit and process silicon on polymer substrates. Typical electronic devices are fabricated on silicon substrates in fabrication lines with process temperatures as high as 1050 °C. These silicon substrates, or wafers, are stiff, brittle, and unusable in a flexible application. The seemingly cheapest substrates for a flexible application are plastics whose maximum processing temperatures are ~150-200 °C. A major factor in the speed of electronic devices is the mobility of the electrons in the semiconducting material. Although single crystal silicon has the highest electron mobility of 650 cm²/V s, polycrystalline silicon thin-film transistors (TFT’s) have reasonably good electron mobility (as high as 500 cm²/V s)¹⁻³ compared to amorphous silicon TFT’s, whose mobility is 2 orders of magnitude lower (1 cm²/V s)⁴. However, direct deposition of amorphous silicon onto polymer substrates can easily be done using various techniques⁵⁻⁷ at sub-150 °C temperatures whereas the typical method to produce polycrystalline films involves solid-phase crystallization⁸ requiring temperatures near 600 °C, and is difficult to process on a limited area. The method to be covered in this paper is a technique developed utilizing an excimer laser to locally crystallize the amorphous silicon that has been deposited on polymer substrates. Because of this novel technique, the polymer does not experience the thermal change that the silicon undergoes. By improving the electron
mobilities, transistors can then be made in this silicon layer with reasonable operating speeds. Although not competitive with CMOS electronics in speed, these thin film transistors are essential in the flexible electronics market.

2. Electron mobility of strained silicon

While the crystalline nature of silicon is very important in determining the electronic mobility in a thin film transistor, it turns out that mechanical strain is also a determining factor in the electron mobility. Although amorphous silicon has a significantly low electron mobility, it is still of interest in flexible electronics and research has gone into determining its resistance to mechanical strain$^{9-11}$. In summary, the research revealed that tensile strain parallel to the film increased the electron mobility of n-type amorphous silicon whereas compressive strain decreased the electron mobility$^{11}$.

Figure 1: Normalized electron field-effect mobility plotted as a function of strain for different TFT's$^{11}$. 
For single-crystal silicon films, the piezoresistance (change in the resistance vs. strain) is a result of the disruption of the cubic symmetry of the crystal\textsuperscript{12}. Stretching in the direction of a crystal plane increases the energy of the conduction band valleys on that axis, transferring the electrons to the other two axis planes conduction valleys. Those transferred electrons now have higher mobility in the directions of the stretched plane. Hole mobility works in the inverse way: resulting in increased mobility in a state of compression.

3. Processing of silicon devices on flexible substrates
3.1. Amorphous silicon deposition

Three methods have been successfully utilized to deposit amorphous silicon on a flexible substrate at low temperatures. These methods include plasma-enhanced chemical vapor deposition (PECVD), phase-vapor deposition (PVD), and low-pressure chemical vapor deposition (LPCVD). While PECVD films are uniform and void-free and extremely useful in an amorphous silicon device (particularly active matrix liquid crystal displays - AMLCD’s), their hydrogen content is typically very high. Pulsed laser crystallization of such a film would result in rapid release and bubbling of the hydrogen within the film and could even lead to film explosion\textsuperscript{13}. However, if the hydrogen levels are limited, there still exists a potential to crystallize the films. PVD and LPCVD films have been found to be immediately useful for laser-crystallization\textsuperscript{14}. 
3.2. Crystallization of silicon on a polymer substrate

Various techniques have been developed to create high-mobility polycrystalline silicon on polymer substrates. Most commonly PVD or LPCVD amorphous silicon films are used as the layer to be laser-crystallized.

The basic mechanism for laser crystallization is outlined in Figure 2 below as extracted from M.O. Thompson’s lecture\(^\text{15}\). The stacked films consist of the plastic substrate, a deposited layer (or two) of barrier SiO\(_2\), and a layer of amorphous silicon with thickness varying from 30 to 300 nm depending on the desired thickness. A pulsed excimer laser (wavelength of 308 nm) is focused onto a spot in the amorphous silicon layer for a duration of approximately 35 ns, turning the amorphous silicon into liquid silicon in the area of the focus. In order to do a full melt (bringing the silicon above its full melt threshold, or FMT), a 100 nm thick amorphous silicon film must be exposed to a fluence of 400 mJ/cm\(^2\) for the pulse duration. Once the pulse of laser light is over, the liquid silicon can solidify into polycrystalline silicon, the duration of which is about 150 ns in total.
The plastic substrate is thermally protected from the silicon by the silicon dioxide barrier/passivation layer. The simulated temperature as a function of time of the various layers can be seen in Figure 3. Although the Si:SiO$_2$ interface experiences roughly the same transient temperature as the silicon itself, it can be observed that the SiO$_2$:polymer interface does not experience this peak temperature. The peak temperature experienced by the polymer is around 200 °C and since this is only for a few tens of microseconds, the polymer is not damaged.
Varying the parameters in the crystallization process can allow tailoring of the polycrystalline grain size. For example, bringing the amorphous silicon only up to a temperature below the full melt threshold will cause only a few seeds to form, resulting in large, 5 \( \mu \text{m} \) size grains (note: grain size is also dependent on film thickness). This large grain size corresponds to a higher electron mobility, resulting in better TFT performance. A pictorial representation of the silicon
seeds at partial melt and full melt, along with AFM images demonstrating grain size for each situation can be seen in Figure 4. 

**Figure 4:** Comparison of grain size by operating at and below the full melt threshold. As can be seen in the figure, operating below the full melt threshold creates larger grain sizes.

Although PECVD films were first avoided for laser-crystallization of the amorphous silicon films due to hydrogen content, the limit of this hydrogen content permissible for laser crystallization as well as a method for dehydrogenation of films above this threshold was explored and demonstrated. Amorphous silicon films deposited by PECVD with 5 at. % and lower could
readily be crystallized into polycrystalline silicon without film explosion or 
additional roughness (see Figure 5).

![AFM images of a 50 nm a-Si:H film after exposure to different pulse energies.](image)

**Figure 5**: AFM images of a 50 nm a-Si:H film after exposure to different pulse energies. (a) a fluence well below the FMT (b) a fluence just below the FMT and (c) a fluence well above the FMT.

For PECVD films with greater than 5 at. % hydrogen all the way up to 10 at. % 
hydrogen, dehydrogenation is performed using low-energy laser irradiation 
before the standard crystallization procedure is performed. These films are 
generally a little rougher than those not requiring the dehydrogenation steps.

Although a high hydrogen content in amorphous silicon films was initially 
considered problematic due to the potential of explosion of the films during laser 
crystalization, scientists discovered a way to exploit this effect in making printed 
polycrystalline silicon films. The approach the scientists took was to first 
deposit amorphous silicon onto a quartz support substrate. The sample was then 
held upside down with respect to the incident laser pulse (see figure 6). The 
major reason for using quartz as opposed to fused silica or some other type of 
substrate is that quartz has low absorption at these short wavelengths (308 nm) 
whereas most glasses have significant absorption at these wavelengths. The
incident laser pulse with the excimer laser melts the amorphous silicon film and
the hydrogen diffuses out of the silicon and up towards the silicon/quartz
interface. As this hydrogen accumulates, pressure builds up in this region and
the polycrystalline silicon that has formed below the hydrogen explodes off of the
wafer and onto the receptor layer below. These droplets coalesce together on the
receptor, creating the patterned polycrystalline film on the new receptor
substrate.

Figure 6: Printed silicon polycrystalline silicon explosion due to hydrogen buildup\textsuperscript{17}.

3.3 Subsequent fabrication steps

After the amorphous or polycrystalline silicon has been deposited on the polymer
substrate, the rest of the fabrication steps must be done to define and create the
TFT. An example series of fabrication steps include deposition of gate oxide and
gate electrode, patterning of the gate, laser doping of source and drain,
patterning silicon regions, deposition of contact isolation oxide, pattern and
etching of isolation oxide, deposition and patterning of metal contacts, and
deposition and patterning of indium-tin oxide (ITO) (see figure 7).
The deposition of the gate oxide can be done using low temperature LPCVD or a low temperature PECVD process. The thickness of this film can be controlled by changing the duration of the deposition process. The next step would be to deposit the metal gate electrode, typically using an electron-beam evaporation technique. This process involves shooting electrons into a crucible of
metals in order to make atoms of metal fly out of the crucible and deposit themselves onto the substrate. This must be done under vacuum in order to achieve the purest metal films possible.

After these two deposition steps, the first photolithographic step must be done to define the gate of the transistor. Typically a photoresist is spun onto the sample, and then exposed to UV light through a glass or quartz mask that has been patterned according to the desired design of the transistor. Within photolithography there is varying freedom regarding feature size and type of exposure used. Typically masks are made whose features are 5 times larger than the final fabricated features. Machines called steppers contain the appropriate UV light source and the corresponding optical components required to create the image that is five times smaller than that printed on the mask. Another method of lithography available for fabrication of electronics is electron-beam lithography. This technique uses a resist that is sensitive specifically to incident electrons. The electron beam tool is programmed to write with the electron beam in the exact pattern desired onto the sample (with electron-beam resist), thereby exposing the resist similar to a photolithography tool. The differences between photolithography and electron beam lithography include a significantly higher resolution for electron beam lithography over the photolithography step. The reason for this is that photolithography is limited by the diffraction limit of the light used to expose the resist. Typically UV or Deep-UV light is used creating a minimum feature size on the order of the wavelength of light. With electron beam lithography, the limiting factor is typically the polymer
chain length in the ebeam resist, which for a typical resist such as PMMA, is around 20 nm.

After the exposure of the resist, the resist is then developed using some kind of chemical developer that removes exposed resist for a positive photoresist, and removes unexposed resist for a negative photoresist. After the removal of the unwanted resist, processes are then done to transfer this pattern into the layers below. In this case the sample will be placed in some kind of environment to remove the metal electrode only where there is no resist to protect it. Following the electrode patterning, the gate oxide is then patterned using either a hydrofluoric acid etch, or reactive ion etching in a CHF$_3$ or CF$_4$ environment.

The next step is to dope the drain and source for the thin film transistor. Since the channel area of the transistor is protected by the multiple layer stack of the gate materials, the doping can be self-aligned. The same excimer laser as used in the crystallization step is used for the doping step. This step is called gas immersion laser doping, or GILD (see figure 8).
After the source and drain have been doped to create the transistor regions, the following steps are all deposition or patterning steps done in a similar fashion as those described above.

4. TFT Performance

Typical TFT on plastic substrate performance is depicted in figure 9 below as I-V curves. The drain-source current as a function of gate-source voltage is shown in the plot on the left and the drain-source current as a function of drain-source voltage is plotted on the right. Both of these curves demonstrate successful TFT performance on a polymer substrate.

Figure 9: Typical I-V curves for a polycrystalline TFT on a plastic substrate."
5. Conclusion

This paper explored the various methods used to deposit and process silicon films on a polymer substrate with the final device being a thin-film transistor. The technology developed by various research groups to achieve these goals has great benefit to the flexible electronic community. Although typical CMOS processing is not immediately applicable to creating flexible electronics, with the new methods described in this paper, flexible electronics can utilize different methods from the CMOS world to create their own integrated flexible thin film transistors.

The creation of TFT’s on polymer substrates is described in great detail including techniques for making amorphous silicon TFT’s or polycrystalline TFT’s. A critical figure of merit for these devices, electron mobility, is compared in the different phases of silicon and when these phases are under mechanical strain; as may readily be seen in a flexible application. The final result is a plot of the transistor performance demonstrating that flexible electronic devices are becoming more of a reality.
References

